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A reduced data bandwidth integrated electrode driver for visual intracortical neural stimulation in 0.35 μm high voltage CMOS

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ABSTRACT

This paper presents an integrated electrode driver for intracortical neural stimulation requiring a reduced data bandwidth. The device has been fabricated in the OnSemi I3T50 0.35 μm high voltage CMOS process, measures 4×4 mm^2 and drives 45 electrodes: electrical measurements corroborate the functional simulations, and confirm that the data bandwidth can be significantly reduced using preloaded wavetables as is introduced in this architecture. The maximum power usage is 13.3 mW under maximum load for all 45 electrodes.

1. Introduction

This work presents an integrated electrode driver aiming to restore a degree of vision in patients suffering from blindness through intracortical stimulation of the visual cortex. It has been reported that points of light, called phosphenes, can be perceived by a subject through electrical stimulation of the visual cortex [1]. Many researchers have successfully elicited phosphenes since 1968 [2–7]. Limitations of these systems have been the efficacy of long term implantation, the practicality of the overall system, the scalability of the implants, the required bandwidth and corresponding power consumption, the stimulation strategy and the number of electrodes that need to be driven [8].

The presented integrated neural stimulator drives 45 electrodes, and requires a very low bandwidth resulting in a reduced power consumption. Since present integrated neural stimulator is intended to be a test platform for multiple types of stimulation strategies, this device is able to operate in monophasic or biphasic modes as well as monopolar or multi-polar modes. Additionally, all 45 electrodes can be driven simultaneously, which provides physiologists a versatile device for experimentation. Present prototype is a wired design: however, architectural decisions have been made on the basis of future versions being wireless. Future versions of the full visual prosthesis will also increase the total number of electrodes from 45 to 630. Past experiments illustrated that an array of 25 by 25 phosphenes is sufficient to provide reading rates between 170 and 100 words per minute depending on whether the text is fixed or scrolled [9].

Because of the natural curvature of the visual cortex, the final visual prosthesis will be split over 14 tiles, with each tile having 45 electrodes that are being controlled and stimulated by a separate wireless neural stimulator chip based on the architecture presented in this paper. Since this multi-tile approach increases the number of implanted devices that simultaneously share and communicate through a single data link, preloaded stimulation patterns, referred to in this paper as wavetables, have been used in order to keep the data rate, and the ensuing power consumption requirements minimal.

This paper is structured as follows. Section 2 presents the general prototype architecture. The philosophy behind the use of prestored and programmable stimulation patterns, identified as wavetables, is described in Section 3. Long term implantation issues have been addressed through the use of a high voltage integration process: it has been reported that stimulation parameters need to be increased beyond initial levels in chronic in vivo trials over time [10], meaning that, in practice, a higher stimulation voltage is required across the electrodes. This system uses high voltage compliant current drivers, and their design is presented in Section 4. Present integrated electrode driver has been implemented in the OnSemi I3T50 0.35 μm process and measures 4×4 mm^2. Electrical measurements corroborate the functional simulations and are shown in Section 5: these confirm that the data rate and corresponding power consumption are significantly reduced using preloaded wavetables as is introduced in this architecture.

2. Integrated neural stimulator architecture

The prototype architecture is shown in Fig. 1: the latter follows a proven approach [8,11–14], but introduces programmable

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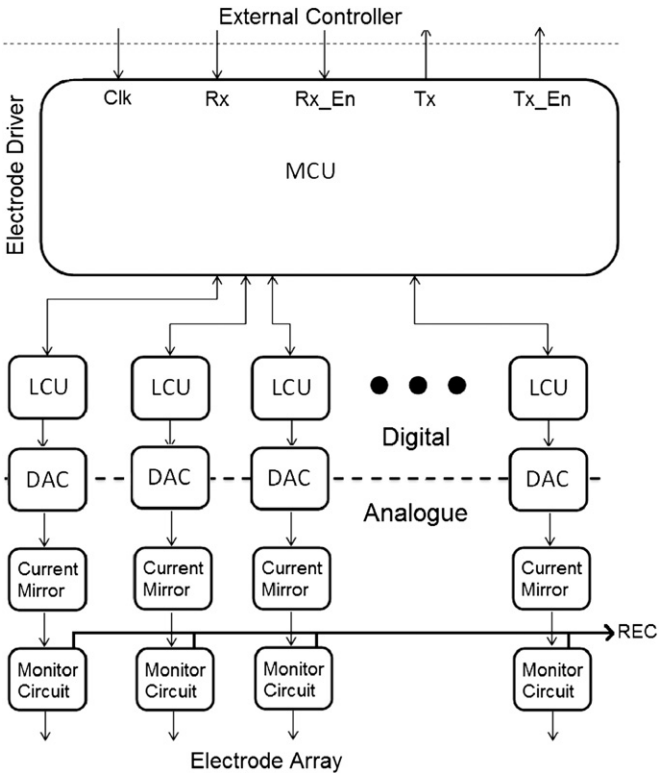

Fig. 1. Prototype architecture.

prestored stimulation patterns, identified as wavetables, which allow to drastically reduce the required data rate. The system has been kept modular so as to be scalable for different numbers of electrodes as well as to mitigate the overall risk, allowing a faulty or underperforming section to be powered down without impacting the remaining circuit operation.

As can be seen in Fig. 1, a central master control unit (MCU) receives the stimulation data, performs error checking and interfaces with local control units (LCU). Each LCU, in turn, stores the wavetables and drives an electrode output stage, which is comprised of a current steering digital to analogue converter (DAC) to create the stimulation pulse. The latter is relayed to a current mirror-type driver so as to allow stimulation current to be sourced to or sinked from the electrode. A monitor circuit records the output stimulus delivered to each electrode, and is used to protect the patient in case of over-current situations as well as to maintain safe operating voltage and current levels on each electrode.

3. Design of the master control unit (MCU)

3.1. Real time stimulation

The digital circuitry communicates with the external controller via a serial interface and controls the shape of the stimulation patterns: the latter are chosen experimentally by physiologists programming the device. The electrode output is controlled via a 6-bit current steering digital to analogue converter (DAC). Although this IC is capable of driving 45 electrodes, the final visual prosthesis requires 630 electrodes, meaning that 14 electrode tiles with a corresponding stimulator chip will be necessary. The required clock speed is limited by the switching speed of the analogue electronics and the expected range of useful stimulation patterns. In order to keep the power consumption minimal, the clock frequency is chosen to be 100 kHz: the ensuing time resolution of the stimulation pulses is equal to 10 μs.

If an external device were to directly control the stimulation waveforms on each of the 630 electrodes in real time, the data rate required for the entire implanted system would be equal to

$$BW_{data} = b \cdot E \cdot f_{clock} = 6 \times 630 \times 100\ \text{kHz} = 378\ \text{MHz}, \quad (1)$$

where f_{clock} is the clock frequency, b is the number of bits quantizing each pixel and E is the number of electrodes. Since this data is intended to be transmitted over a wireless link, an error checking overhead would also need to be included which would increase the required data rate even more, resulting in an unpractically high requirement. The latter is particularly a problem as the carrier frequency should ideally be kept below a few MHz due to the electromagnetic power absorption in the tissue at higher frequencies: it has been reported that above a few MHz, the conductivity of the human body increases dramatically, which means that more energy is absorbed, while below the MHz range, the inductors receiving the wireless power and data need to have unpractical large values [15]. Beyond approximately 100 MHz, the skin depth decreases steeply meaning that the attenuation increases significantly. For these reasons, higher data bandwidths are not necessarily achieved at higher carrier frequencies, and almost all reported systems with data rates exceeding 2 Mbps operate with carrier frequencies below 100 MHz [16]. Consequently, the obtained data rate in (1) is not a practical value, compared to the data rates that are obtained in state of the art wireless neural stimulators [8,11,17,18] and recorders [19].

3.2. Wavetables

The data rate can be reduced by pre-programming the electrode stimulation patterns on the chip. To "turn on" a phosphene, the device needs to stimulate a particular electrode with this stimulation pattern, identified as a wavetable. The latter are stored in the device's volatile memory when the device is powered on. After all the wavetables have been programed into the device, each new frame needs to either turn on or off these patterns. Using epiretinal stimulation, phosphene flicker has been reported to be eliminated at a stimulation rate of 40–50 Hz [20]: in the presented neural stimulator, the frame rate is kept high (100 Hz) in order to allow for raster scans of electrode as well as simultaneous or bipolar stimulation while still operating at a rate that is acceptable for the patient. The number of phosphenes that can be elicited simultaneously will be obtained through future in vivo measurements.

The minimum bandwidth required by previously described system is significantly lower compared to a real time transmission scheme, and can be calculated using the following expression:

$$BW_{data} = n \cdot E \cdot f_{frame}, \quad (2)$$

where f_{frame} is the frame frequency, n is the number of bits required to represent the amount stored wavetables per electrode in a binary format, and E is the number of electrodes. As can be seen, the net benefit of previously described system is to reduce the required bandwidth by trading the clock frequency for the frame frequency, and by prestoring on-chip the stimulation patterns that are applied to each electrode, instead of transmiting the data in real time. Although this architecture allows multiple wavetables per electrode output (resulting in grey scale like images), only one wavetable is stored per electrode in present prototype as a proof of concept. Consequently, this means that at a frame rate of 100 Hz, the minimum bandwidth required by this strategy is 63 kbps for 630 electrodes. If redundancy for error checking is included at 30% overhead, then the data rate is below

100 kbps, which is the intended bandwidth for the ongoing inductive link design.

When the device is switched on, or when it is being reprogrammed, the external device loads the wavetables into the MCU. These wavetables are then used until the device is either switched off or new wavetables are loaded from the external controller. In each frame rate period, data is sent to the device to indicate which electrodes are to be stimulated with their wavetables and which ones are not: these wavetables will be tuned so that the patient will observe a phosphene when an electrode is turned on. Admittedly, the required stimulus data will change over time and additionally, the wavetables will be wiped from the internal memory each time the chip is unpowered or reset. In both cases, they need to be, respectively, reprogrammed by the caretaker or reloaded from the external unit's memory. However, it is important to note that this reprogramming is not a real time operation, and does not, therefore, form a time critical design parameter in this architecture.

3.3. Stimulation patterns

The stimulating patterns used in this system are comprised of a burst of biphasic or monophasic electrical pulses emitted within a defined time period, as reported in [12]. The time resolution is set by the clock frequency, and is therefore equal to 10 μs: the wavetable format is shown in Fig. 2. The stimulation is controlled via the modification of the following parameters: A_{an}, A_{cat} (anodic/cathodic pulse quantized level), T_1, T_3 (width of cathodic/anodic pulse), T_2 (width between an anodic and subsequent cathodic pulse or vice versa), T_4 (delay between two biphasic pulses in one frame), T_5 (delay at the end of a frame during which the electrode is left unstimulated) and N (number of biphasic pulses in one frame). There is also a single bit that indicates whether the burst starts with an anodic or a cathodic phase, allowing bipolar stimulation with the intention of multiple electrodes sourcing and sinking current of the same magnitude. Monophasic stimulation is obtained by zeroing the amplitude and the width of the wanted cathodic or anodic pulse.

3.4. Patient safety

An incorrectly programed wavetable can cause more damage than a single erroneous point of direct electrode control. For this reason, error checking is crucial. Commands sent to the implanted electronics are divided into packets of data and nested cyclic redundancy checks are used to detect errors. This version of the device can also be interrogated to retrieve the currently loaded wavetables. The bandwidth required to drive a single device incorporating error checking is currently 12.1 kbps. Increasing the number of electrodes can reduce the relative size of header overhead: in this stimulator prototype, the redundancy has been chosen to be larger than 30% so that there are less architectural changes as electrode numbers increase. Moreover, the monitor circuit records the output stimulus delivered to each electrode and is used to maintain safe operating voltage and current levels on each electrode.

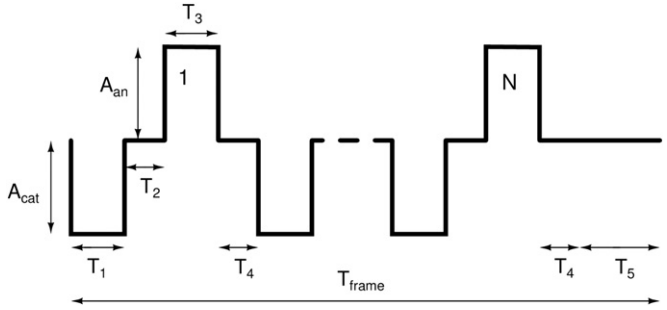

Fig. 2. The format of a stimulation pattern.

4. Electrode output driver design

The most common strategy for electrical neural stimulation is charge balanced, constant current biphasic pulses, as these tend to cause less neuronal loss than monophasic pulses [10]. Constant current stimulation has the advantage of more easily controlling charge injection as electrode impedances change over time. Threshold currents (i.e. the currents at which neuronal stimulation occurs) are dependent on electrode geometry which, in turn, affects the impedance of the electrodes [21]. Similar designs reported threshold currents to be between 1.9 μA and 96 μA [4,5]. Based on early experimental tests with prototype electrodes, an electrode impedance of 100 kΩ forms the upper limit of electrode impedance in present system: therefore, an upper current limit of approximately 90 μA was chosen, resulting in an maximum supply voltage compliance of 20 V, as the outputs need to source and sink the electrode current. This explains why a high voltage technology was used to fabricate the device so as to allow the output driver to operate at 20 V, while the MCU, LCU's and DAC's operate at the core voltage (3.3 V).

The electrode output circuit is shown in Fig. 3. This stage is very similar to reported current output amplifiers [13, 14, 22, 23], and uses high voltage devices to ensure an increased voltage compliance. The supply voltages V_{DD} and $-V_{SS}$ are set to 10 V and −10 V, respectively. The circuit contains a 6-bit current steering DAC which is controlled by the corresponding LCU. The output of the DAC is buffered and amplified through a current mirror (M_{n1-3}). The mirrored current ratio between M_{n1}, M_{n2}, M_{n3} and M_{p1}, M_{p2} is 1:1:8 and 1:8, respectively, so as to reduce the power consumption.

High voltage transistors (M_{nhv1-3} and M_{phv1-2}) are used to drive the output current to each electrode, while M_{nhv4} and M_{phv3} are high voltage switches that determine the polarity of the stimulation current (sourcing or sinking). This topology allows for a higher voltage compliance of the constant current outputs, while maintaining an improved matching owing to the use of low voltage current mirror transistors (M_{n1-3} and M_{p1-2}). Transistor M_{nhv3} ensures that self-biased cascode transistors can be used, which simplifies the overall design. While no high voltage is dropped across M_{nhv1} and M_{phv1}, they are realized as high voltage devices so as to match with M_{nhv2} and M_{phv2}, respectively, as well as to simplify the latter's biasing. The LCU provides the *HI*/*LO* signals turning on/off M_{nhv4} and M_{phv3}, determining whether current is sourced or sinked in an electrode. The signal *HI* is level

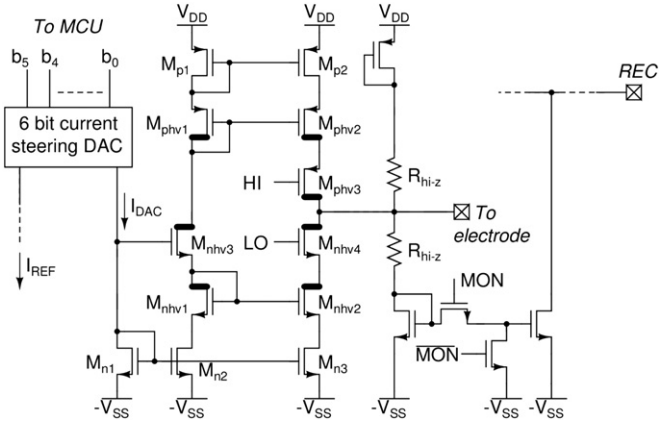

Fig. 3. Electrode output and monitoring circuit.

shifted such that the maximal gate source voltage of M_{phv2} is not exceeded: signal *LO* does not require level shifting as the integrated stimulators common ground is connected to the $-V_{SS}$ terminal. In the case of monopolar stimulation, a return electrode is maintained external to the device at patient ground potential.

A high impedance voltage divider ($R_{hi-z} = 1\ \mathrm{M\Omega}$) is included to allow monitoring of the voltage across each electrode. The current through the NMOS current mirror at the lower potential of the voltage divider implies the voltage on the electrode, since the value of R_{hi-z} is known by design. A PMOS diode-connected transistor is added so as to keep the voltage divider symmetric. The output nodes (*REC*) of the monitoring NMOS current mirrors are connected together so only one terminal is required to observe the electrodes: this topology uses sequential but dynamical monitoring, which reduces the pin count. By providing an external pull up resistor connected to terminal *REC*, the voltage across each electrode can be measured without a direct electrical connection to the electrode. One electrode is selected for monitoring using the digital $MON/\overline{MON}$ signals, provided by the LCU's. The transistors and switches have been designed so as to shield the output electrodes optimally from each other without injecting interferences. Observation of the *REC* potential reveals whether the device is operating within or outside its voltage compliance. The ratio of the electrode voltage to *REC* is dependent on the value of the pull up transistor and the potential it is pulled to, meaning that a one-time calibration is required. The corresponding measurement results are presented in the next section.

The output impedance is affected by the presence of the monitoring voltage divider circuit, since a small portion of the electrode current is sensed by the monitoring circuit. Charge balanced cathodic and anodic pulses are also disturbed by the former's presence: since perfectly charge balanced pulses are not achievable in practice [10], the resistors will correct the remaining charge after the stimulation is complete. Matching between the two R_{hi-z} resistors in each output stage is critical, as mismatch between them will cause a net charge pumping, resulting in a potential difference between the electrode and the ground: both have been lay-outed as interdigitized sections so as to match very closely [24]. The PMOS and NMOS diode-connected transistors were carefully dimensioned as well so as to drop the same gate source voltage. This has been ascertained using extensive simulations, and has been confirmed with measurements. Finally, a patient ground return electrode is set at a potential that is the average measured across six electrodes when these are not stimulated. The resulting maximum potential difference has been measured and the results are explained in next section.

5. Measurement results

The neural integrated stimulator has been fabricated in the OnSemi I3T50 0.35 μm high voltage CMOS process: a microphotograph of the device is shown in Figs. 4 and 5. The size of the die is $4 \times 4\ \mathrm{mm}^2$. The neural stimulator chip has been connected to a test PCB, which is driven by an FPGA board. The latter uploads specific testing wavetables to the prototype after power up, and drives transmit and recording commands to the IC. Functional and automatic test pattern testing confirmed the functional operation of the neural stimulator prototype. No significant cross talk between electrodes has been measured.

5.1. Electrode output measurements

The output voltage across an electrode with an impedance of 100 kΩ has been measured for all DAC codes: this measurement is shown in Fig. 6. The resulting differential and integral nonlinearity errors are 140 mV and 195 mV, respectively. The voltage

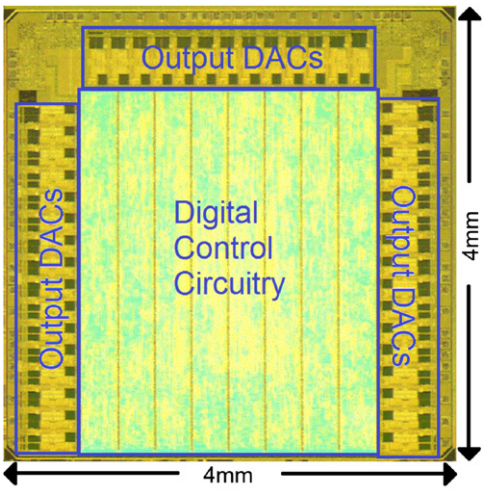

Fig. 4. Microphotograph of the integrated neural stimulator.

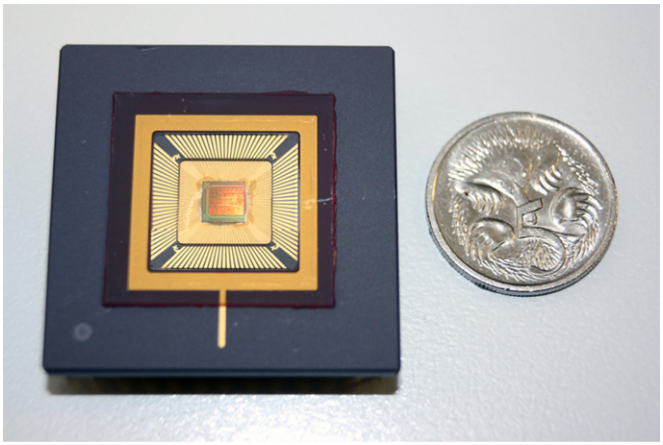

Fig. 5. Packaged sample being measured in the electrical lab.

compliance of this circuit during testing was 17.3 V. The least significant bit voltage for this load is 270 mV. Given these conditions, the patient ground return electrode is set at 9.25 V above the minimum potential, which is enforced by the external circuitry.

The mismatch of the monitoring voltage divider circuits has been measured relative to the derived patient ground potential. This mismatch results in a maximum potential difference of ± 10 mV across all stages when the output drivers are off. The source and sinking electrode currents between different outputs match within 13%. For monopolar stimulation, a one-time calibration is required so as to ensure that the accumulated net charge is minimal. When the device is to be used for bipolar stimulation, then the individual devices must first be characterised so that DAC control inputs can compensate for current mismatch between electrodes, meaning that the currents need to match within 2.7 μA (1 LSB). The resistors R_{hi-z} provide a return path, and an extra mitigation against charge accumulation. Since electrode impedances are complex and nonlinear, future in vivo tests are planned to determine what current flows when electrodes are not stimulating. It is expected that these results are going to be dependent on the electrodes and the composition of the electrolytic substrate.

5.2. Electrode monitoring results

It is important that the electrode monitor line accurately represents a scaled version of the electrode potential. Fig. 7 shows a sample stimulation pattern with the monitor output scaled: it

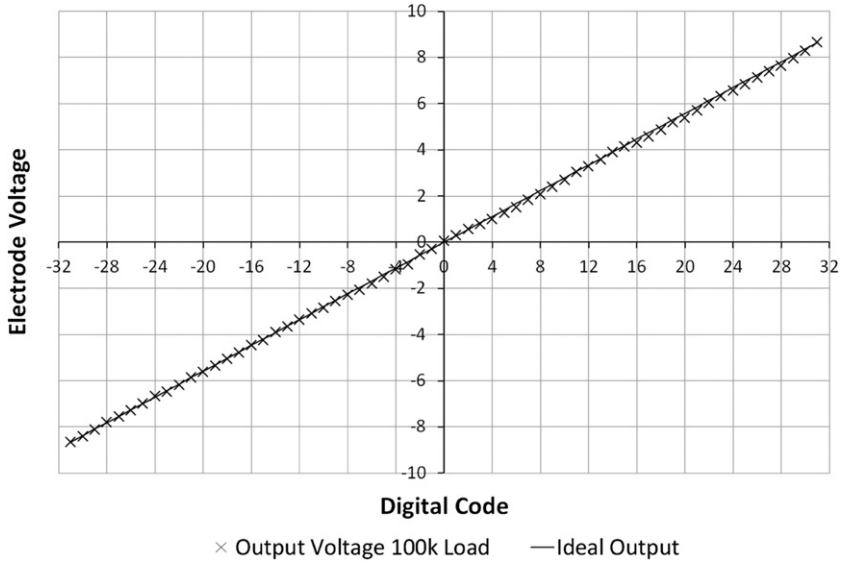

Fig. 6. Electrode output for all DAC codes.

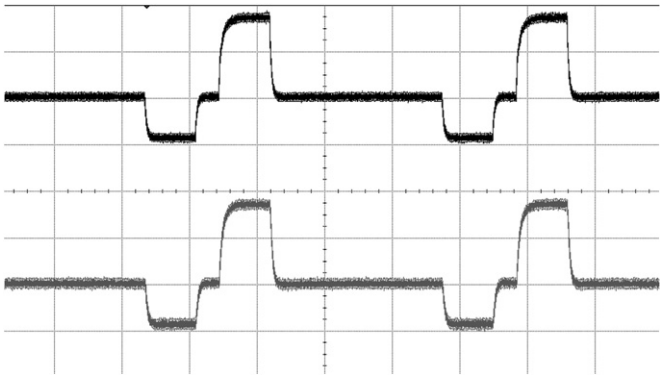

Fig. 7. Monitoring the circuit output. The upper waveform is the monitor inverted electrode output. The lower waveform is the monitor circuit output. The lower waveform is scaled to 5 V per division while the upper waveform is 600 mV per division. The timescale is 200 μs per division.

can be seen that the monitored output is an accurate representation of the electrode voltage. The ratio of the electrode voltage to *REC* is dependent on the value of the pull up transistor and the potential it is pulled to: in present test implementation, this ratio is 12:1.

5.3. Power consumption measurements

The power consumption was measured under a heavy bipolar stimulation load: the digital circuitry requires approximately 1 mA of current while the output drivers require 0.5 mA. This brings the total power usage to approximately 13.3 mW in case all 45 electrodes are being driven under a maximal load. As observed in the measurements, the power consumption of the neural stimulator chip is defined by the stimulating pattern. Ongoing animal studies will confirm whether the presence of more electrodes will decrease individual maximum stimulating currents.

6. Conclusion

This paper presents the design of an integrated electrode driver for visual intracortical neural stimulation. It has been illustrated that the data bandwidth can be significantly reduced using preloaded wavetables as is introduced in this architecture. This circuit has been designed in the OnSemi I3T50 0.35 μm high voltage CMOS process. Measurements corroborate the functional simulations and confirm the correct operation of the device: the maximum power usage is 13.3 mW under maximum load for all 45 electrodes.

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