The solid line in Fig. 3 is the theoretical slope that would be expected from a thermally limited system. That not even the 0.5kHz curve has the correct slope we attribute to timing jitter and word length effects. The measured BER curves approach to within ±0.1 dB of the thermally limited slope as the word length is decreased to 16 bits. The lower frequency limit of the receiver is about 50 kHz, which should cause no problems even for a 2^16 PRBS. That the laser is completely free of MPN was checked by BER measurements over 12.5 km.

The actual value of the bias penalty (2.2 dB) obtained in this experiment is probably determined by the bias tee in combination with imperfections of the BER generator. Both the BER generator (Anritusu MP 1701A), the bias tee, and the laser (14-MQW-DFB) are designed for 10 Gbit/s operation and their performance when characterised in pure SOG systems is excellent. This shows that even top quality equipment used over only a part of its nominal bandwidth has enough variation in amplitude and phase response to create serious problems for wide bandwidth signals such as a 2^11 PRBS.

Different lasers have widely different chirp noise characteristics. The amount of timing jitter, which is closely related to the chirp noise, should depend on the laser resonance frequency and the sidemode suppression [5, 7]. This is indeed the case in our measurements where the lasers with the highest relaxation frequency and lowest sidemode suppression show the least chirp noise. The laser used here has a low relaxation frequency and a high sidemode suppression of over 40 dB, giving it the most severe chirp noise problems, appearing already at 37.5 km. Even if the chirp noise is not seen directly in oscilloscope measurements, it is often visible as a degradation in the BER performance at long distance.

Conclusions: The chirp noise originates in the spontaneous emission noise below threshold, and is thus a fundamental effect. It can be avoided by driving the laser above threshold at all times. It may give a BER floor at medium distances (≥ 40 km) in dispersive links at Gbit/s data rates. Owing to the improvement in typical drive circuitry, the bias power necessary to ascertain that the laser is always above threshold can be significant, and may correspond to an optical power penalty of 1-2 dB.

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References


UP TO 16 dB IMPROVEMENT IN DETECTED VOLTAGE USING TWO-SECTION SEMICONDUCTOR OPTICAL AMPLIFIER DETECTOR

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Indexing terms: Optical detectors, Optical amplifiers

A semiconductor optical amplifier detector with an improved responsivity, obtained using two contacts is demonstrated. It is shown that up to 16 dB improvement in detected output voltage may be obtained for a semiconductor optical amplifier with an internal gain of 30 dB. Initial experimental results showing a 4 dB improvement are presented.

Introduction: There is much interest in the use of semiconductor optical amplifiers (SOAs) to amplify optical signals while simultaneously detecting the signal [1–4]. Applications include use as a lossless ‘tap’ [1], for header extraction in photonic packet switching [2], as a broadband network controller [3], and for optical regeneration [4]. One limitation of the devices considered for these applications is the relatively low output impedance and voltage levels compared to pin diodes with high impedance levels. We demonstrate a significant improvement in the detector responsivity of an SOA by dividing the contact into two sections.

Theory: Light input into an SOA causes stimulated emission resulting in a change in the carrier density [1]. The relation between the change in photon density ΔP(z) at a distance z along the cavity from the input facet and the change in carrier density ΔN(z) can be obtained from the standard rate equation for carrier density [5] as

\[ \Delta N(z) = -\Delta S(z) \mu_p q \]  

(1)

where ΔN(z) is the change in carrier density at any point z along the length of the SOA, ΔS(z) is the change in photon density at the same point, τp is the carrier lifetime, q is the charge of an electron, and N is the steady state carrier density. For small ΔN(z) the change in voltage is directly proportional to the change in carrier density and thus is directly proportional to the change in photon density.

If an optical amplifier has a single electrical contact along the entire length of the device and is operated below saturation, the optical intensity increases exponentially as it propagates along the length of the SOA. If the amplifier length is L and the net gain coefficient is g = g - g_m, where g_m is the attenuation coefficient, the internal optical gain is exp (gL). Given an input photon density ΔS_m the output photon density is given by ΔS_o = ΔS_m exp (gL). The contact voltage generated by a change in photon density is proportional to the average of ΔV below the contact. By integrating along the length of the device, it is easy to show that the average is

\[ \Delta V_{\text{contact}} = \Delta S_m k T q \exp (gL) - 1 \]  

(2)

where k is a constant.

The detector response can be improved by dividing the electrical contact into two sections. The first section of the SOA acts as an optical preamplifier and the second section acts as a detector. This is illustrated in Fig. 1, which shows a two-section amplifier with contacts of length L_s and L_d. Note that, unlike previous work on integrated optical preamplifiers (e.g. Reference 6) where the output of the preamplifier is absorbed by a photodiode, the detector section in the present device acts as an amplifier and allows the optical signal to pass through the two-section amplifier.
The voltage on the second contact is the gain of the first section \( g' \), multiplied by the average of \( \Delta V' \) under the second contact. Following the argument above this average is

\[
\Delta V_{\text{second}} = \Delta S \exp \left( \frac{g' L_1}{L_2} \right) \left( \exp \left( \frac{g' L_1}{L_2} - 1 \right) \right)
\]

Comparing the output voltages of a one-section SOA to a two-section SOA, the improvement in responsivity obtained from the two-section SOA, for \( \exp \left( \frac{g' L_1}{L_2} \right) \), is

\[
\text{improvement (dB)} = 20 \log_{10} \left( \frac{\Delta V_{\text{second}}}{\Delta V_{\text{one-section}}} \right)
\]

\[
= 20 \log_{10} \left( \frac{(L_1 + L_2)[1 - \exp \left( -\frac{g' L_2}{L_2} \right)]}{L_2} \right)
\]

**Optimisation of contact length:**

Eqn. 5 implies that the length of the second contact \( L_2 \) should be minimised for maximum improvement. However, the impedance of the second contact is an important consideration. To obtain a large detection bandwidth the load impedance connected to the second contact should be relatively low. A 50Ω microwave amplifier was used in these calculations. For an input optical signal modulated with a 100 MHz square wave was coupled into the SOA, using a tapered, lensed, single-mode fibre. The output was collected with a similar fibre. The bias currents through the contacts were chosen to give equal current density in the two sections with a total bias current of 200 mA. The input power was –12 dBm and the fibre-to-fibre gain of the device was measured to be 4 dB. The detected signal voltage was extracted with a RF bias tee, electrically amplified and displayed on a sampling oscilloscope. Fig. 3 shows the detected signal. Fig. 3a gives the detected signal voltage from a single contact SOA by electrically connecting the two contacts with a small bondwire. Fig. 3b shows the detected voltage with only the second contact used as a detector with both contacts supplied with bias current. The improvement in detected signal amplitude is 4dB. This is in good agreement with the results shown in Fig. 2b which predict an improvement of 5dB for a 400μm long device with an internal gain of 10dB.

**Conclusion:** We have demonstrated theoretically and experimentally that the detected signal voltage from a semiconductor optical amplifier increased with the SOA length and the improvement in detector responsivity was approximately proportional to the ratio of the internal optical gains of 10 and 30dB. The best calculated improvement in output voltage is about 16dB.
A CMOS Manchester adder based on precharge/discharge dynamic techniques [1] provides speed and density advantages over static adders for VLSI implementation in a high speed arithmetic unit. Using the BiCMOS dynamic Manchester carry look ahead circuit, a 16-bit full adder test circuit which has been designed based on a 2-μm BiCMOS technology, shows a more than two times improvement in speed as compared to the CMOS Manchester carry look ahead circuit. The speed advantage of the BiCMOS dynamic carry look ahead circuit is even greater in a 32-bit or 64-bit adder, which is very helpful for high-speed VLSI CPU designs.

Introduction: A CMOS Manchester adder based on precharge/discharge dynamic techniques [1] provides speed and density advantages over static adders for VLSI implementation in arithmetic circuits. The speed performance of the CMOS dynamic Manchester adder is mainly determined by the pass-transistor-related ripple-carry propagation delay [2]. For a large scale arithmetic circuit, this pass-transistor-related ripple-carry propagation delay limits the overall speed performance in an ALU circuit. In addition, extra inverters are needed in the full adder circuit using the Manchester carry look ahead scheme. In this Letter, a faster BiCMOS dynamic carry look ahead circuit, which is built by cascading BiCMOS dynamic logic gates without race problems, is described.

BiCMOS dynamic carry look ahead circuit: Fig. 1 shows the new 4-bit BiCMOS dynamic MCLA circuit in two pairs of N- and P-type BiCMOS MCLA cells. The output of each BiCMOS MCLA cell, the carry signal, is taken as the input to another cell. To shorten the precharge/predischarge time, BiCMOS precharge/predischarge circuits have been used in every cell. As in a pipelined system, cascading dynamic logic gates may cause serious race problems [3]. In the new BiCMOS dynamic MCLA circuit, race problems have been avoided by placing the 'complementary' BiCMOS dynamic MCLA cells as shown in Fig. 1 alternatively in the MCLA circuit. In the N-type cells as shown in Fig. 1, the BiCMOS circuit, which is composed of the bipolar transistor Q3 and MOS transistors MP and MN, has been used as the precharge circuit. In the N cell, initially, during the precharge period as defined by the CK signal, the output node is precharged to a high voltage, close to 5V. During the precharge period, the pull-down bipolar transistor Q3 is turned off by the BiCMOS precharge circuit. During the logic evaluation period, the output node is determined by the BiCMOS logic gate. To avoid race problems, in each N or P cell, one transition state is prohibited at the input. Specifically, in the N cell, inputs cannot have a transition state from 0 to 5V. In addition, the N and P cells are placed alternatively in the MCLA such that the output of an N(P)-cell and is also the input to a P(N)-cell. After the precharge/predischarge period, the output is set high. During the logic evaluation period, if inputs A and B are low and input C is initially high, the output node is discharged via the BiCMOS logic gate. After C settles to its logic level 0, the output voltage may be already at a low state. Because it is a dynamic circuit, the output cannot be pulled high again at this moment. An error state is thus created. Similarly, in the P cell, inputs cannot have a transition state from 0 to 5V. In addition, the N and P cells are placed alternatively in the BiCMOS dynamic MCLA circuit such that the output of an N(P)-cell and is also the input to a P(N)-cell. After the precharge/predischarge period, in the BiCMOS dynamic MCLA, each internal output node is set high and low alternatively. With this arrangement, race problems are successfully avoided in our circuit.

Speed performance and discussion: To evaluate the performance of the BiCMOS dynamic MCLA circuit, a test chip including two 16-bit full adders using the BiCMOS and CMOS dynamic MCLA circuits has been designed based on a 2-μm BiCMOS technology. Fig. 2 shows the layout of two 16-bit full adders using CMOS and BiCMOS dynamic MCLA circuits. As shown in the centre region of both test chips, the 16-bit BiCMOS dynamic MCLA circuit occupies an area of 184 × 713 μm², which is about 30% larger as compared to the CMOS circuit, which has an area of 219 × 459 μm². Fig. 3 shows the transient waveforms of the carry signals C4, C6, C12 and C16 in the 16-bit CMOS and BiCMOS dynamic circuits.