The solid line in Fig. 3 is the theoretical slope that would be expected from a thermally limited system. That not even the 0 km curve has the correct slope we attribute to timing jitter and word length effects. The measured BER curves approach to within $\pm 0{\cdot}1$ dB of the thermally limited slope as the word length is decreased to 16 bits. The lower frequency limit of the receiver is about 50 kHz, which should cause no problems even for a 2^{31} PRBS. That the laser is completely free of MPN was checked by BER measurements over 12·5 km.

The actual value of the bias penalty (2·2 dB) obtained in this experiment is probably determined by the bias tee in combination with imperfections of the BER generator. Both the BER generator (Anritsu MP 1701A), the bias tee, and the laser ($\lambda/4$-MQW-DFB) are designed for 10 Gbit/s operation and their performance when characterised in pure 50 Ω systems is excellent. This shows that even top quality equipment used over only a part of its nominal bandwidth has enough variation in amplitude and phase response to create serious problems for wide bandwidth signals such as a 2^{31} PRBS.

Different lasers have widely different chirp noise characteristics. The amount of timing jitter, which is closely related to the chirp noise, should depend on the laser resonance frequency and the sidemode suppression [5, 7]. This is indeed the case in our measurements where the lasers with the highest relaxation frequency and lowest sidemode suppression show the least chirp noise. The laser used here has a low relaxation frequency and a high sidemode suppression of over 40 dB, giving it the most severe chirp noise problems, appearing already at 37 km. Even if the chirp noise is not seen directly in oscilloscope measurements, it is often visible as a degradation in the BER performance at long distance.

Conclusions: The chirp noise originates in the spontaneous emission noise below threshold, and is thus a fundamental effect. It can be avoided by driving the laser above threshold at all times. It may give a BER floor at medium distances (≥ 40 km) in dispersive links at Gbit/s data rates. Owing to the imprecision in typical drive circuitry, the bias power necessary to ascertain that the laser is always above threshold can be significant, and may correspond to an optical power penalty of 1–2 dB.

4th November 1991

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UP TO 16 dB IMPROVEMENT IN DETECTED VOLTAGE USING TWO-SECTION SEMICONDUCTOR OPTICAL AMPLIFIER DETECTOR

R. M. Fortenberry, A. J. Lowery and R. S. Tucker

Indexing terms: Optical detectors, Optical amplifiers

A semiconductor optical amplifier detector with an improved responsivity, obtained using two contacts is demonstrated. It is shown that up to 16 dB improvement in detected output voltage may be obtained for a semiconductor optical amplifier with an internal gain of 30 dB. Initial experimental results showing a 4 dB improvement are presented.

Introduction: There is much interest in the use of semiconductor optical amplifiers (SOAs) to amplify optical signals while simultaneously detecting the signal [1–4]. Applications include use as a lossless 'tap' [1], for header extraction in photonic packet switching [2], as a broadband network controller [3], and for optical regeneration [4]. One limitation of the devices considered for these applications is the relatively low output impedance and voltage levels compared to *pin* diodes with high impedance levels. We demonstrate a significant improvement in the detector responsivity of an SOA by dividing the contact into two sections.

Theory: Light input into an SOA causes stimulated emission resulting in a change in the carrier density [1]. The relation between the change in photon density $\Delta S(z)$ at a distance z along the cavity from the input facet and the change in carrier density $\Delta N(z)$ can be obtained from the standard rate equation for carrier density [5] as

$$\Delta N(z) = -\Delta S(z) t_s g v_g \tag{1}$$

where $\Delta N(z)$ is the change in carrier density at any point z along the length of the SOA, $\Delta S(z)$ is the change in photon density at the same point, t_s is the carrier lifetime, g is the material gain per unit length, and v_g is the group velocity within the amplifier.

The change in junction voltage $\Delta V(z)$ at a point z on the junction is given by [5]

$$\Delta V(z) = \eta\left(\frac{kT}{q}\right) \ln\left[\frac{N + \Delta N(z)}{N}\right] \tag{2}$$

where η is the junction ideality factor, k is the Boltzman constant, T is temperature, q is the charge of an electron, and N is the steady state carrier density. For small $\Delta N(z)$ the change in voltage is directly proportional to the change in carrier density and thus is directly proportional to the change in photon density.

If an optical amplifier has a single electrical contact along the entire length of the device and is operated below saturation, the optical intensity increases exponentially as it propagates along the length of the SOA. If the amplifier length is L and the net gain coefficient is $g' = g - \alpha_{sc}$, where α_{sc} is the attenuation coefficient, the internal optical gain is exp $(g'L)$. Given an input photon density ΔS_{in}, the output photon density is given by $\Delta S_{out} = \Delta S_{in}$ exp $(g'L)$. The contact voltage generated by a change in photon density is proportional to the average of ΔV below the contact. By integrating along the length of the device, it is easy to show that this average is

$$\Delta V_{1\text{-section}} = \Delta S_{in} K\left[\frac{\exp(g'L) - 1}{g'L}\right] \tag{3}$$

where K is a constant.

The detector response can be improved by dividing the electrical contact into two sections. The first section of the SOA acts as an optical preamplifier and the second section acts as a detector. This is illustrated in Fig. 1, which shows a two-section amplifier with contacts of length L_1 and L_2. Note that, unlike previous work on integrated optical preamplifiers (e.g. Reference 6) where the output of the preamplifier is absorbed by a photodiode, the detector section in the present device acts as an amplifier and allows the optical signal to pass through the two-section amplifier.

The voltage on the second contact is the gain of the first section exp $(g'L_1)$, multiplied by the average of ΔV under the second contact. Following the argument above this average is

$$\Delta V_{2\text{-section}} = \Delta S_{in} K \exp(g'L_1)\left[\frac{\exp(g'L_2) - 1}{g'L_2}\right] \quad (4)$$

Comparing the output voltages of a one-section SOA to a two-section SOA, the improvement in responsivity obtained from the two-section SOA, for $\exp(g'L) \gg 1$, is

$$\text{improvement (dB)} = 20 \log_{10}\left(\frac{\Delta V_{2\text{-section}}}{\Delta V_{1\text{-section}}}\right)$$

$$= 20 \log_{10}\left\{\frac{(L_1 + L_2)[1 - \exp(-g'L_2)]}{L_2}\right\} \quad (5)$$

Optimisation of contact length: Eqn. 5 implies that the length of the second contact L_2 should be minimised for maximum improvement. However, the impedance of the second contact is an important consideration. To obtain a large detection bandwidth the load impedance connected to the second contact should be relatively low. A 50Ω microwave amplifier input impedance would be suitable in many applications.

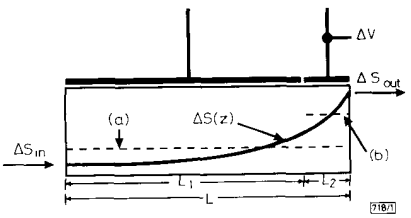

Fig. 1 *Diagram of two section semiconductor optical amplifier showing change in photon density along length*

– – – – photon density average (*a*) over total length $L_1 + L_2$, and (*b*) over second contact L_2

Note that the contact resistance of the contact on an SOA is inversely proportional to its length. A longer contact is desirable to reduce the series contact resistance whereas a shorter contact is needed to improve the detector responsivity as indicated above. Thus the optimum contact length is a compromise between these two competing demands.

The optimum length for the second contact can be determined by modelling the SOA detector as a simple circuit. The model consists of a low impedance forward-biased junction connected in series with a resistor, representing the contact resistance, whose value is inversely proportional to the length of the second contact as described above. The load impedance of the electrical amplifier is connected in series. Note that increasing the length of the second contact decreases the contact resistance and increases the detected voltage obtained across the load impedance. Fig. 2 shows the detected voltage and improvement in responsivity, calculated using this simple circuit model combined with eqns. 1 and 2 above. An SOA having an internal gain of 30dB, an impedance of 1·0Ω, a length of 1000μm, and an input optical power of −30dBm is used in these calculations. Fig. 2*a* shows the calculated change in detected voltage against length of second contact for the second contact connected to electrical amplifiers with 50Ω and 1MΩ input impedances. The optimum length of the second electrode is shown to be about 70μm. It is important to note that such a large impedance as 1MΩ may not be practical in some applications due to limitations on bandwidth.

From eqn. 5, the improvement in detector responsivity is roughly proportional to the ratio $(L_1 + L_2)/L_2$. In addition, the contact resistance decreases as the second contact is lengthened. Thus increasing the total length of the device $(L_1 + L_2)$ allows the second section to be sufficiently long to give a relatively low contact resistance while keeping the ratio $(L_1 + L_2)/L_2$ large. Fig. 2*b* shows the improvement in detector response as a function of the total length of the SOA for internal optical gains of 10 and 30dB. The best calculated improvement in output voltage is about 16dB.

Experimental results: To test the above predictions the detector response of a two section SOA was measured. The optical amplifier consisted of a 1·3μm InGaAsP device with two contacts. The first contact was 315μm long and the second contact was 90μm long with a 20μm gap between the contacts. The forward-biased resistance of the device with both contacts in parallel was measured to be 2·5Ω.

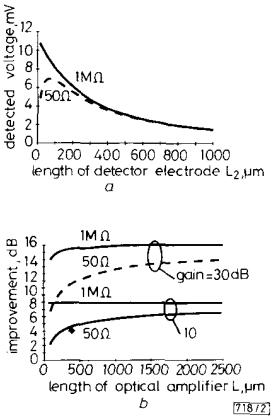

Fig. 2 *Calculations of detected voltage against length of second contact and improvement in detector responsivity against length of optical amplifier for internal optical gains of 10 and 30dB, and load impedances of 50Ω and 1MΩ*

● Experimental result

a Detected voltage against length of second contact

b Improvement in detector responsivity against length of optical amplifier

An input optical signal modulated with a 100MHz square wave was coupled into the SOA using a tapered, lensed, singlemode fibre. The output was collected with a similar fibre. The bias currents through the contacts were chosen to give equal current density in the two sections with a total bias current of 200mA. The input power was −12dBm and the fibre-to-fibre gain of the device was measured to be 3dB. The detected signal voltage was extracted with a RF bias tee, electrically amplified and displayed on a sampling oscilloscope. Fig. 3 shows the detected signal. Fig. 3*a* gives the detected response of the device used as a single contact SOA by electrically connecting the two contacts with a small bondwire. Fig. 3*b* shows the detected voltage with only the second contact used as a detector with both contacts supplied with bias current. The improvement in detected signal amplitude is 4dB. This is in good agreement with the results shown in Fig. 2*b* which predict an improvement of 5dB for a 400μm long device with an internal gain of 10dB.

Conclusion: We have demonstrated theoretically and experimentally that the detected signal voltage from a semicon-

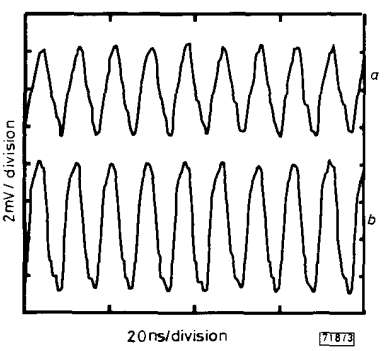

Fig. 3 *Detected voltage from both contacts and second contact only*

a Both contacts

b Second contact only

ductor optical amplifier can be significantly improved by splitting the contact into two separate contacts. Calculations indicate that 16 dB improvement is possible with 30 dB internal gain. Experimental results using an unoptimised device show a 4 dB improvement in good agreement with the calculated value of 5 dB.

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BiCMOS DYNAMIC MANCHESTER CARRY LOOK AHEAD CIRCUIT FOR HIGH SPEED ARITHMETIC UNIT VLSI

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Indexing terms: Large-scale integration, Integrated circuits

A new BiCMOS dynamic Manchester carry look ahead circuit is presented, which is free from race problems, for VLSI implementation in a high speed arithmetic unit. Using the BiCMOS dynamic Manchester carry look ahead circuit, a 16 bit full adder test circuit which has been designed based on a 2 μm BiCMOS technology, shows a more than two times improvement in speed as compared to the CMOS Manchester carry look ahead circuit. The speed advantage of the BiCMOS dynamic carry look ahead circuit is even greater in a 32 bit or 64 bit adder, which is very helpful for high speed VLSI CPU designs.

Introduction: A CMOS Manchester adder based on precharge/discharge dynamic techniques [1], provides speed and density advantages over static adders for VLSI implementation of arithmetic circuits. The speed performance of the CMOS dynamic Manchester adder is mainly determined by the pass-transistor-related ripple-carry propagation delay [2]. For a large scale arithmetic circuit, this pass-transistor-related ripple-carry propagation delay limits the overall speed performance in an ALU circuit. In addition, extra inverters are needed in the full adder circuit using the Manchester carry look ahead scheme. In this Letter, a faster BiCMOS dynamic carry look ahead circuit, which is built by cascading BiCMOS dynamic logic gates without race problems, is described.

BiCMOS dynamic carry look ahead circuit: Fig. 1 shows the new 4 bit BiCMOS dynamic MCLA circuit in two pairs of *N*- and *P*-type BiCMOS MCLA cells. The output of each BiCMOS MCLA cell, the carry signal, is taken as the input to another cell. To shorten the precharge/predischarge time, BiCMOS precharge/predischarge circuits have been used in every cell. As in a pipelined system, cascading dynamic logic gates may cause serious race problems [3]. In the new BiCMOS dynamic MCLA circuit, race problems have been avoided by placing the 'complementary' BiCMOS dynamic MCLA cells as shown in Fig. 1 alternatively in the MCLA circuit. In the *N*-type cells as shown in Fig. 1, the Bi*p*MOS circuit, which is composed of the bipolar transistor Q_1 and MOS transistors MP_1 and MN_5, has been used as the precharge circuit. In the *N* cell, initially, during the precharge period as defined by the CK signal, the output node is precharged to a high voltage, close to 5 V. During the precharge period, the pull-down bipolar transistor Q_2 is turned off by turning on the MOS transistor MN_4. A logic evaluation period follows the precharge period. During this period, the Bi*p*MOS precharge circuit is turned off and the output voltage is determined by the Bi*n*MOS logic gate including the MOS transistors MN_1, MN_2, MN_3 and the bipolar transistor Q_2. As shown in Fig. 1, the *P*-type cell has a complementary characteristic. During the predischarge period, its output node is discharged to close to 0 V by the Bi*n*MOS predischarge circuit. During the logic evaluation period, the output is determined by the Bi*p*MOS logic gate. To avoid race problems, in each *N* or *P* cell, one transition state is prohibited at the input. Specifically, in the *N* cell, inputs cannot have a transition state from 5 to 0 V because the output may be accidentally switched to an incorrect state. In the *N* cell, after the precharge period, the output is set high. During the logic evaluation period, if inputs A and B are low and input C is initially high, the output node is discharged via the Bi*n*MOS logic gate. After C settles to its logic level −0 V, the output voltage may be already at a low state. Because it is a dynamic circuit, the output cannot be pulled high again at this moment. An error state is thus created. Similarly, in the *P* cell, inputs cannot have a transition state from 0 to 5 V. In addition, the *N* and *P* cells are placed alternatively in the BiCMOS dynamic MCLA circuit such that the output of an *N*(*P*)-cell and is also the input to a *P*(*N*)-cell. After the precharge/predischarge period, in the BiCMOS dynamic MCLA, each internal output node is set high and low alternatively. With this arrangement, race problems are successfully avoided in our circuit.

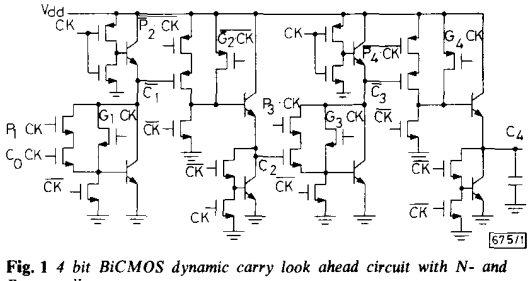

Fig. 1 *4 bit BiCMOS dynamic carry look ahead circuit with N- and P-type cells*

Speed performance and discussion: To evaluate the performance of the BiCMOS dynamic MCLA circuit, a test chip including two 16 bit full adders using the BiCMOS and CMOS dynamic MCLA circuits has been designed based on a 2 μm BiCMOS technology. Fig. 2 shows the layout of two 16 bit full adders using CMOS and BiCMOS dynamic MCLA circuits. As shown in the centre region of both test chips, the 16 bit BiCMOS dynamic MCLA circuit occupies an area of 184 × 713 μm^2, which is about 30% larger as compared to the CMOS circuit, which has an area of 219 × 459 μm^2. Fig. 3 shows the transient waveforms of the carry signals C_4, C_8, C_{12} and C_{16} in the 16 bit CMOS and BiCMOS dynamic