A Low-Power FSK Modulator/Demodulator for an MICS Band Transceiver

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Abstract — This paper presents a low-power FSK (Frequency Shift Keying) modulator/demodulator. It supports a data rate of 20 kb/s and uses a phase interpolating clock recovery circuit that forces the rising edge of the clock track the demodulated data precisely. In the transmitter side, the base-band data directly modulate a four stage differential ring VCO (Voltage Controlled Oscillator) with an FSK tone frequency of 80 kHz fitting into one of ten 300-kHz channels allocated at the new 402-405 MHz MICS (Medical Implant Communication Services) band. The designs are implemented in a 0.18-µm CMOS process. The all digital demodulator circuits consume only 33.41 µA current from a 1.5-V supply.

Index Terms — Voltage-controlled oscillator, Frequency Shift Keying.

I. INTRODUCTION

The design of very low power, implantable data telemetry chips to record physiological parameters from a patient body is becoming very important, considering the comfort such devices can provide to the patient. This paper describes a new and less complex FSK modulator/demodulator scheme for a single chip 402-405 MHz direct conversion transceiver. The challenges associated with full integration and the general specifications for the proposed transceiver were discussed in [1]. Since the biological signals are mostly low-bandwidth signals (ECG 0.05 to 256 Hz, EEG 0.05 to 128 Hz, EOG 0.1 to 64 Hz, EMG 1 to 1000 Hz, Neural 200 to 2400 Hz, Blood flow DC to 100 Hz, Blood Pres. DC to 100 Hz), the sensor interface circuit of the target implantable device requires the transceiver be able to handle a data rate of 20 kb/s. The block diagram of the transceiver is shown in Fig. 1.

II. DIRECT MODULATION OF THE VCO IN TRANSMIT MODE

In the transmit mode, the PLL loop opens and the base-band data directly modulates the four stage differential ring VCO to save power. Although it has higher phase noise compared to an LC tank oscillator, ring option was evaluated because of its low power consumption. An appropriate choice of FSK tone frequency can relieve the phase noise requirement of the VCO [1]. In order to minimize the center frequency variations in transmit mode, the VCO gain should be kept very low. However, having a narrow tuning range might leave the ring VCO frequency range out of the desired band, considering the effect of process variations. To prevent this to happen, a second static calibration loop is utilized to keep the VCO frequency in the desired range, as shown in Fig. 2. Every delay cell in this VCO gets three bit calibration control and two bit FSK control signals. These two bit FSK data turn long channel devices M11 and M12 on and off, causing the total sink current change in slight amounts such that frequency deviations will be around 80 kHz.

The VCO including the buffers and the driver amplifiers is fabricated in TSMC 0.18-µm CMOS process before incorporating it into the PLL loop. The measured spectrum and the tuning characteristics of this ring VCO is shown in Fig. 3. The VCO with buffers consumes 738 µA current from a 1.5 V supply providing the desired overlapping linear tuning clusters.
Although an average frequency deviation of $\pm 120\,\text{kHz}$ observed with FSK control, the device has shown poor frequency stability. The measured frequency peak was moving with more than 40 kHz offset from the desired center frequency due to the noise on the supply and the control lines. This drawback associated with this ring VCO should be addressed in order to be able to observe accurate 80 kHz FSK tones.

### III. ALL DIGITAL BASEBAND

The baseband consists of a data demodulator and a simple clock recovery circuit. The demodulator part is an improved version of classic Vance demodulator. In a Vance demodulator, the hard limited I and Q signals are fed into a simple D-type flip-flop to obtain the baseband data [2]. Although very simple in implementation, this scheme exhibits poor BER (Bit Error Rate) performance in the case of a low SNR (Signal to Noise Ratio) at the demodulator input.

The block diagram of the proposed data demodulation and clock recovery circuit is shown in Fig. 4. In the data demodulator block, I and Q signals first pass through a DSP block to remove the glitches generated by feeding the noisy quadrature signals into the hard limiters. After this simple DSP stage, clean quadrature signals are fed into a D-type flip-flop to recover the baseband data. The circuits corresponding to both approaches were emulated in Matlab to compare the BER performances. The BER plots are depicted in Fig. 5. For low SNR values, this preprocessing approach outperforms the only D-Flipflop case. Shifting into the high SNR regions, the BER plots start to converge, a result that can be expected intuitively. Although BER values at these
plots would not reflect the precise circuit outcomes, they clearly show the performance improvement due to a simple DSP step. The detailed waveforms of the digital demodulator are depicted in Fig. 6a. The sinusoidal quadrature components I and Q are converted to the digital domain by two limiter amplifiers. These signals are then sampled by a reference clock, which is the PLL’s 3.14-MHz reference clock already available in the system. Then, the digital comparator compares the total number of samples and decides whether it is less or bigger than zero. Thus, the glitches in the \( X_I \) and \( X_Q \) are eliminated. The output of the comparator is either “1” or “0” within pulse duration \( T_I \), as indicated in Fig. 6a.

Having the data without glitches and errors during the corresponding bit period relieves the design of clock recovery circuit. Regarding the clock recovery block, the four phases of the 20-kHz clock (obtained by dividing 3.14-MHz PLL reference clock) are used to assure that the rising edge of the clock hits the midrange of the data period [3]. This is done by checking the time difference between the rising edges of the data and the clock. Depending on the difference, the leading or lagging phase is selected to move the rising edge to the midrange. The waveforms illustrating the operation are shown in Fig. 6b. For such a phase interpolation scheme, it is optimum to have the switching thresholds set at a quarter of the full data period away from the edges. For such a choice, the data recovery block should assure no more than a \( \%25 \) variations in the data period. In practice, the baseband data frequency difference, and the phase difference between the received carrier and the LO (Local Oscillator) frequency would cause variations in the demodulated bit period. It can be shown that the worst case variation would correspond to one full FSK tone period. For this reason, a full period of FSK tone should be kept less than a quarter of full data period for reliable operation. This leaves us with a minimum 80-kHz FSK tone frequency to handle a data rate of 20 kb/s.

The phase switching timing circuits should assure smooth phase transitions in order not to introduce any glitch during the transitions which would mean to sample the same data twice. For this reason, the timing for switching to a leading clock phase is asymmetric with respect to the timing for switching to a lagging clock phase. The simulated waveforms show that the clock can track the mid-range of the demodulated data for both increasing and decreasing data periods without sampling the same data bit twice (Fig. 7).
IV. CONCLUSION

A less complex FSK modulator/demodulator circuits have been designed in 0.18-μm CMOS process to be used in a fully integrated MICS band transceiver. The measured current consumption of the self calibrating differential ring VCO with FSK modulation is only 738μA from a 1.5-V supply. Simulations show that the implemented DSP for the baseband processing that includes data demodulation and clock recovery circuits consumes a current of 33.41 μA which is extremely low.

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