

RFM22B/23B REGISTER DESCRIPTIONS

1. Complete Register Summary

Table 1. Register Descriptions

Add	R/W	Function/Desc	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
00	R	Device Type	0	0	0	dt[4]	dt[3]	dt[2]	dt[1]	dt[0]	00111
01	R	Device Version	0	0	0	vc[4]	vc[3]	vc[2]	vc[1]	vc[0]	06h
02	R	Device Status	ffovfl	ffunfl	rxfem	headerr	reserved	reserved	cps[1]	cps[0]	—
03	R	Interrupt Status 1	ifferr	itxffaull	itxffaem	irxffaull	iext	ipksent	ipkvalid	icrcerror	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	entxffaull	entxffaem	enrxffaull	enext	enpkjent	enpvalid	enrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	03h
07	R/W	Operating & Function Control 1	swres	enlbd	enwt	x32ksel	txon	rxon	pllon	xton	01h
08	R/W	Operating & Function Control 2	antdiv[2]	antdiv[1]	antdiv[0]	rxmpk	autotx	enldm	ffclrrx	ffclrtx	00h
09	R/W	Crystal Oscillator Load Capacitance	xtalshft	xlcl[6]	xlcl[5]	xlcl[4]	xlcl[3]	xlcl[2]	xlcl[1]	xlcl[0]	7Fh
0A	R/W	Microcontroller Output Clock	Reserved	Reserved	clkt[1]	clkt[0]	enlfc	mclk[2]	mclk[1]	mclk[0]	06h
0B	R/W	GPIO0 Configuration	gpio0drv[1]	gpio0drv[0]	pup0	gpio0[4]	gpio0[3]	gpio0[2]	gpio0[1]	gpio0[0]	00h
0C	R/W	GPIO1 Configuration	gpio1drv[1]	gpio1drv[0]	pup1	gpio1[4]	gpio1[3]	gpio1[2]	gpio1[1]	gpio1[0]	00h
0D	R/W	GPIO2 Configuration	gpio2drv[1]	gpio2drv[0]	pup2	gpio2[4]	gpio2[3]	gpio2[2]	gpio2[1]	gpio2[0]	00h
0E	R/W	I/O Port Configuration	Reserved	extitst[2]	extitst[1]	extitst[0]	itsdo	dio2	dio1	dio0	00h
0F	R/W	ADC Configuration	adcstart/adc-done	adcsl[2]	adcsl[1]	adcsl[0]	adcref[1]	adcref[0]	adcgain[1]	adcgain[0]	00h
10	R/W	ADC Sensor Amplifier Offset	Reserved	Reserved	Reserved	Reserved	adcoffs[3]	adcoffs[2]	adcoffs[1]	adcoffs[0]	00h
11	R	ADC Value	adc[7]	adc[6]	adc[5]	adc[4]	adc[3]	adc[2]	adc[1]	adc[0]	—
12	R/W	Temperature Sensor Control	tsrange[1]	tsrange[0]	entsoffs	entstrim	tstrim[3]	tstrim[2]	tstrim[1]	tstrim[0]	20h
13	R/W	Temperature Value Offset	tvofts[7]	tvofts[6]	tvofts[5]	tvofts[4]	tvofts[3]	tvofts[2]	tvofts[1]	tvofts[0]	00h
14	R/W	Wake-Up Timer Period 1	Reserved	Reserved	Reserved	wtr[4]	wtr[3]	wtr[2]	wtr[1]	wtr[0]	03h
15	R/W	Wake-Up Timer Period 2	wtm[15]	wtm[14]	wtm[13]	wtm[12]	wtm[11]	wtm[10]	wtm[9]	wtm[8]	00h
16	R/W	Wake-Up Timer Period 3	wtm[7]	wtm[6]	wtm[5]	wtm[4]	wtm[3]	wtm[2]	wtm[1]	wtm[0]	01h
17	R	Wake-Up Timer Value 1	wtv[15]	wtv[14]	wtv[13]	wtv[12]	wtv[11]	wtv[10]	wtv[9]	wtv[8]	—
18	R	Wake-Up Timer Value 2	wtv[7]	wtv[6]	wtv[5]	wtv[4]	wtv[3]	wtv[2]	wtv[1]	wtv[0]	—
19	R/W	Low-Duty Cycle Mode Duration	ldc[7]	ldc[6]	ldc[5]	ldc[4]	ldc[3]	ldc[2]	ldc[1]	ldc[0]	00h
1A	R/W	Low Battery Detector Threshold	Reserved	Reserved	Reserved	lbd[4]	lbd[3]	lbd[2]	lbd[1]	lbd[0]	14h
1B	R	Battery Voltage Level	0	0	0	vbat[4]	vbat[3]	vbat[2]	vbat[1]	vbat[0]	—
1C	R/W	IF Filter Bandwidth	dwn3_bypass	ndec[2]	ndec[1]	ndec[0]	filset[3]	filset[2]	filset[1]	filset[0]	01h
1D	R/W	AFC Loop Gearshift Override	afcbd	enafc	afcgearh[2]	afcgearh[1]	afcgearh[0]	1p5 bypass	matap	ph0size	40h
1E	R/W	AFC Timing Control	swait_timer[1]	swait_timer[0]	shwait[2]	shwait[1]	shwait[0]	await[2]	await[1]	await[0]	0Ah
1F	R/W	Clock Recovery Gearshift Override	Reserved	Reserved	crfast[2]	crfast[1]	crfast[0]	crslow[2]	crslow[1]	crslow[0]	03h
20	R/W	Clock Recovery Oversampling Ratio	rxosr[7]	rxosr[6]	rxosr[5]	rxosr[4]	rxosr[3]	rxosr[2]	rxosr[1]	rxosr[0]	64h
21	R/W	Clock Recovery Offset 2	rxosr[10]	rxosr[9]	rxosr[8]	stallctrl	ncoff[19]	ncoff[18]	ncoff[17]	ncoff[16]	01h
22	R/W	Clock Recovery Offset 1	ncoff[15]	ncoff[14]	ncoff[13]	ncoff[12]	ncoff[11]	ncoff[10]	ncoff[9]	ncoff[8]	47h
23	R/W	Clock Recovery Offset 0	ncoff[7]	ncoff[6]	ncoff[5]	ncoff[4]	ncoff[3]	ncoff[2]	ncoff[1]	ncoff[0]	AEh

Table 1. Register Descriptions (Continued)

Add	R/W	Function/Desc	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
24	R/W	Clock Recovery Timing Loop Gain 1	Reserved	Reserved	Reserved	rxncocomp	crgain2x	crgain[10]	crgain[9]	crgain[8]	02h
25	R/W	Clock Recovery Timing Loop Gain 0	crgain[7]	crgain[6]	crgain[5]	crgain[4]	crgain[3]	crgain[2]	crgain[1]	crgain[0]	8Fh
26	R	Received Signal Strength Indicator	rss[7]	rss[6]	rss[5]	rss[4]	rss[3]	rss[2]	rss[1]	rss[0]	—
27	R/W	RSSI Threshold for Clear Channel Indicator	rssith[7]	rssith[6]	rssith[5]	rssith[4]	rssith[3]	rssith[2]	rssith[1]	rssith[0]	1Eh
28	R	Antenna Diversity Register 1	adrssia[7]	adrssia[6]	adrssia[5]	adrssia[4]	adrssia[3]	adrssia[2]	adrssia[1]	adrssia[0]	—
29	R	Antenna Diversity Register 2	adrssib[7]	adrssib[6]	adrssib[5]	adrssib[4]	adrssib[3]	adrssib[2]	adrssib[1]	adrssib[0]	—
2A	R/W	AFC Limiter	Afclim[7]	Afclim[6]	Afclim[5]	Afclim[4]	Afclim[3]	Afclim[2]	Afclim[1]	Afclim[0]	00h
2B	R	AFC Correction Read	afc_corr[9]	afc_corr[8]	afc_corr[7]	afc_corr[6]	afc_corr[5]	afc_corr[4]	afc_corr[3]	afc_corr[2]	00h
2C	R/W	OOK Counter Value 1	afc_corr[9]	afc_corr[9]	ookfrzen	peakdeten	madeten	ookcnt[10]	ookcnt[9]	ookcnt[8]	18h
2D	R/W	OOK Counter Value 2	ookcnt[7]	ookcnt[6]	ookcnt[5]	ookcnt[4]	ookcnt[3]	ookcnt[2]	ookcnt[1]	ookcnt[0]	BCh
2E	R/W	Slicer Peak Hold	Reserved	attack[2]	attack[1]	attack[0]	decay[3]	decay[2]	decay[1]	decay[0]	26h
2F	Reserved										
30	R/W	Data Access Control	enpacrx	lsbfrst	crconly	skip2ph	enpactx	encrc	crc[1]	crc[0]	8Dh
31	R	EzMAC status	0	rxrcr1	pkscrch	pkrx	pkvalid	crcerror	pktx	pkstent	—
32	R/W	Header Control 1	bcen[3:0]				hdch[3:0]				0Ch
33	R/W	Header Control 2	skipsyn	hdlen[2]	hdlen[1]	hdlen[0]	fixklen	syncden[1]	syncden[0]	prealen[8]	22h
34	R/W	Preamble Length	prealen[7]	prealen[6]	prealen[5]	prealen[4]	prealen[3]	prealen[2]	prealen[1]	prealen[0]	08h
35	R/W	Preamble Detection Control	preath[4]	preath[3]	preath[2]	preath[1]	preath[0]	rss[off][2]	rss[off][1]	rss[off][0]	2Ah
36	R/W	Sync Word 3	sync[31]	sync[30]	sync[29]	sync[28]	sync[27]	sync[26]	sync[25]	sync[24]	2Dh
37	R/W	Sync Word 2	sync[23]	sync[22]	sync[21]	sync[20]	sync[19]	sync[18]	sync[17]	sync[16]	D4h
38	R/W	Sync Word 1	sync[15]	sync[14]	sync[13]	sync[12]	sync[11]	sync[10]	sync[9]	sync[8]	00h
39	R/W	Sync Word 0	sync[7]	sync[6]	sync[5]	sync[4]	sync[3]	sync[2]	sync[1]	sync[0]	00h
3A	R/W	Transmit Header 3	txhd[31]	txhd[30]	txhd[29]	txhd[28]	txhd[27]	txhd[26]	txhd[25]	txhd[24]	00h
3B	R/W	Transmit Header 2	txhd[23]	txhd[22]	txhd[21]	txhd[20]	txhd[19]	txhd[18]	txhd[17]	txhd[16]	00h
3C	R/W	Transmit Header 1	txhd[15]	txhd[14]	txhd[13]	txhd[12]	txhd[11]	txhd[10]	txhd[9]	txhd[8]	00h
3D	R/W	Transmit Header 0	txhd[7]	txhd[6]	txhd[5]	txhd[4]	txhd[3]	txhd[2]	txhd[1]	txhd[0]	00h
3E	R/W	Transmit Packet Length	pklen[7]	pklen[6]	pklen[5]	pklen[4]	pklen[3]	pklen[2]	pklen[1]	pklen[0]	00h
3F	R/W	Check Header 3	chhd[31]	chhd[30]	chhd[29]	chhd[28]	chhd[27]	chhd[26]	chhd[25]	chhd[24]	00h
40	R/W	Check Header 2	chhd[23]	chhd[22]	chhd[21]	chhd[20]	chhd[19]	chhd[18]	chhd[17]	chhd[16]	00h
41	R/W	Check Header 1	chhd[15]	chhd[14]	chhd[13]	chhd[12]	chhd[11]	chhd[10]	chhd[9]	chhd[8]	00h
42	R/W	Check Header 0	chhd[7]	chhd[6]	chhd[5]	chhd[4]	chhd[3]	chhd[2]	chhd[1]	chhd[0]	00h
43	R/W	Header Enable 3	hden[31]	hden[30]	hden[29]	hden[28]	hden[27]	hden[26]	hden[25]	hden[24]	FFh
44	R/W	Header Enable 2	hden[23]	hden[22]	hden[21]	hden[20]	hden[19]	hden[18]	hden[17]	hden[16]	FFh
45	R/W	Header Enable 1	hden[15]	hden[14]	hden[13]	hden[12]	hden[11]	hden[10]	hden[9]	hden[8]	FFh
46	R/W	Header Enable 0	hden[7]	hden[6]	hden[5]	hden[4]	hden[3]	hden[2]	hden[1]	hden[0]	FFh
47	R	Received Header 3	rxhd[31]	rxhd[30]	rxhd[29]	rxhd[28]	rxhd[27]	rxhd[26]	rxhd[25]	rxhd[24]	—
48	R	Received Header 2	rxhd[23]	rxhd[22]	rxhd[21]	rxhd[20]	rxhd[19]	rxhd[18]	rxhd[17]	rxhd[16]	—
49	R	Received Header 1	rxhd[15]	rxhd[14]	rxhd[13]	rxhd[12]	rxhd[11]	rxhd[10]	rxhd[9]	rxhd[8]	—
4A	R	Received Header 0	rxhd[7]	rxhd[6]	rxhd[5]	rxhd[4]	rxhd[3]	rxhd[2]	rxhd[1]	rxhd[0]	—
4B	R	Received Packet Length	rxplen[7]	rxplen[6]	rxplen[5]	rxplen[4]	rxplen[3]	rxplen[2]	rxplen[1]	rxplen[0]	—
4C-4E	Reserved										
4F	R/W	ADC8 Control	Reserved	Reserved	adc8[5]	adc8[4]	adc8[3]	adc8[2]	adc8[1]	adc8[0]	10h
50-5F	Reserved										
60	R/W	Channel Filter Coefficient Address	inv_pre_th[3]	inv_pre_th[2]	inv_pre_th[1]	inv_pre_th[0]	chfiladd[3]	chfiladd[2]	chfiladd[1]	chfiladd[0]	00h

Table 1. Register Descriptions (Continued)

Add	R/W	Function/Desc	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
61			Reserved								
62	R/W	Crystal Oscillator/Control Test	pwst[2]	pwst[1]	pwst[0]	clkhyst	enbias2x	enamp2x	bufovr	enbuf	24h
63-68			Reserved								
69	R/W	AGC Override 1	Reserved	sgi	agcen	lnagain	pga3	pga2	pga1	pga0	20h
6A-6C			Reserved								
6D	R/W	TX Power	papeakval	papeaken	papeaklv[1]	papeaklv[0]	lna_sw	txpow[2]	txpow[1]	txpow[0]	18h
6E	R/W	TX Data Rate 1	txdr[15]	txdr[14]	txdr[13]	txdr[12]	txdr[11]	txdr[10]	txdr[9]	txdr[8]	0Ah
6F	R/W	TX Data Rate 0	txdr[7]	txdr[6]	txdr[5]	txdr[4]	txdr[3]	txdr[2]	txdr[1]	txdr[0]	3Dh
70	R/W	Modulation Mode Control 1	Reserved	Reserved	txdtrscale	enphwpdn	manppol	enmaninv	enmanch	enwhite	0Ch
71	R/W	Modulation Mode Control 2	trclk[1]	trclk[0]	dtmod[1]	dtmod[0]	eninvs	fd[8]	modtyp[1]	modtyp[0]	00h
72	R/W	Frequency Deviation	fd[7]	fd[6]	fd[5]	fd[4]	fd[3]	fd[2]	fd[1]	fd[0]	20h
73	R/W	Frequency Offset 1	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	fo[9]	fo[8]	00h
75	R/W	Frequency Band Select	Reserved	sbsel	hbssel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	75h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h
78			Reserved								
79	R/W	Frequency Hopping Channel Select	fhch[7]	fhch[6]	fhch[5]	fhch[4]	fhch[3]	fhch[2]	fhch[1]	fhch[0]	00h
7A	R/W	Frequency Hopping Step Size	fhs[7]	fhs[6]	fhs[5]	fhs[4]	fhs[3]	fhs[2]	fhs[1]	fhs[0]	00h
7B			Reserved								
7C	R/W	TX FIFO Control 1	Reserved	Reserved	txafthr[5]	txafthr[4]	txafthr[3]	txafthr[2]	txafthr[1]	txafthr[0]	37h
7D	R/W	TX FIFO Control 2	Reserved	Reserved	txaethr[5]	txaethr[4]	txaethr[3]	txaethr[2]	txaethr[1]	txaethr[0]	04h
7E	R/W	RX FIFO Control	Reserved	Reserved	rxafthr[5]	rxafthr[4]	rxafthr[3]	rxafthr[2]	rxafthr[1]	rxafthr[0]	37h
7F	R/W	FIFO Access	fifod[7]	fifod[6]	fifod[5]	fifod[4]	fifod[3]	fifod[2]	fifod[1]	fifod[0]	—

AN440

2. Detailed Register Descriptions

Register 00h. Device Type Code (DT)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			dt[4:0]				
Type	R					R		

Reset value = 00001000

Bit	Name	Function
7:5	Reserved	Reserved.
4:0	dt[4:0]	Device Type Code. EZRadioPRO: 01000.

Register 01h. Version Code (VC)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			vc[4:0]				
Type	R					R		

Reset value = xxxxxxxx

Bit	Name	Function
7:5	Reserved	Reserved.
4:0	vc[4:0]	Version Code. Code indicating the version of the chip. Rev B1: 00110.

Register 02h. Device Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ffovfl	ffunfl	rxffem	headerr	Reserved	Reserved	cps[1:0]	
Type	R	R	R	R	R	R	R	

Reset value = xxxxxxxx

Bit	Name	Function
7	ffovfl	RX/TX FIFO Overflow Status.
6	ffunfl	RX/TX FIFO Underflow Status.
5	rxffem	RX FIFO Empty Status.
4	headerr	Header Error Status. Indicates if the received packet has a header check error.
3:2	Reserved	Reserved.
1:0	cps[1:0]	Chip Power State. 00: Idle State 01: RX State 10: TX State

Register 03h. Interrupt/Status 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ifferr	itxffafull	itxffaem	irxffafull	iext	ipksent	ipkvalid	icrcerror
Type	R	R	R	R	R	R	R	R

Reset value = xxxxxxxx

Bit	Name	Function
7	ifferr	FIFO Underflow/Overflow Error. When set to 1 the TX or RX FIFO has overflowed or underflowed.
6	itxffafull	TX FIFO Almost Full. When set to 1 the TX FIFO has met its almost full threshold and needs to be transmitted.
5	itxffaem	TX FIFO Almost Empty. When set to 1 the TX FIFO is almost empty and needs to be filled.
4	irxffafull	RX FIFO Almost Full. When set to 1 the RX FIFO has met its almost full threshold and needs to be read by the microcontroller.
3	iext	External Interrupt. When set to 1 an interrupt occurred on one of the GPIO's if it is programmed so. The status can be checked in register 0Eh. See GPIOx Configuration section for the details.
2	ipksent	Packet Sent Interrupt. When set to 1 a valid packet has been transmitted.
1	ipkvalid	Valid Packet Received. When set to 1 a valid packet has been received.
0	icrcerror	CRC Error. When set to 1 the cyclic redundancy check is failed.

When any of the Interrupt/Status 1 bits change state from 0 to 1 the device will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 1 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 1 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

Table 2. Interrupt or Status 1 Bit Set/Clear Description

Bit	Status Name	Set/Clear Conditions
7	ifferr	Set if there is a FIFO overflow or underflow. Cleared by applying FIFO reset.
6	itxffaull	Set when the number of bytes written to TX FIFO is greater than the Almost Full threshold. Automatically cleared at the start of transmission when the number of bytes in the FIFO is less than or equal to the threshold.
5	itxffaem	Set when the number of bytes in the TX FIFO is less than or equal to the Almost Empty threshold. Automatically cleared when the number of data bytes in the TX FIFO is above the Almost Empty threshold.
4	irxffaull	Set when the number of bytes in the RX FIFO is greater than the Almost Full threshold. Cleared when the number of bytes in the RX FIFO is below the Almost Full threshold.
3	iext	External interrupt source.
2	ipksent	Set once a packet is successfully sent (no TX abort). Cleared upon leaving FIFO mode or at the start of a new transmission.
1	ipkvalid	Set up the successful reception of a packet (no RX abort). Cleared upon receiving and acknowledging the Sync Word for the next packet.
0	icrcerror	Set if the CRC computed from the RX packet differs from the CRC in the TX packet. Cleared at the start of reception for the next packet.

Table 3. When are Individual Status Bits Set/Cleared if not Enabled as Interrupts?

Bit	Status Name	Set/Clear Conditions
7	ifferr	Set if there is a FIFO Overflow or Underflow. It is cleared only by applying FIFO reset to the specific FIFO that caused the condition.
6	itxffaull	Will be set when the number of bytes written to TX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we start transmitting and the FIFO data is read out and the number of bytes left in the FIFO is smaller or equal to the threshold).
5	itxffaem	Will be set when the number of bytes (not yet transmitted) in TX FIFO is smaller or equal than the Almost Empty threshold set by SPI. It is automatically cleared when we write enough data to TX FIFO so that the number of data bytes not yet transmitted is above the Almost Empty threshold.
4	irxffaull	Will be set when the number of bytes received (and not yet read-out) in RX FIFO is greater than the Almost Full threshold set by SPI. It is automatically cleared when we read enough data from RX FIFO so that the number of data bytes not yet read is below the Almost Full threshold.
3	iext	External interrupt source
2	ipksent	Will go high once a packet is sent all the way through (no TX abort). This status will be cleaned if 1) We leave FIFO mode or 2) In FIFO mode we start a new transmission.
1	ipkvalid	Goes high once a packet is fully received (no RX abort). It is automatically cleaned once we receive and acknowledge the Sync Word for the next packet.
0	icrcerror	Goes High once the CRC computed during RX differs from the CRC sent in the packet by the TX. It is cleaned once we start receiving new data in the next packet.

AN440

Register 04h. Interrupt/Status 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor
Type	R	R	R	R	R	R	R	R

Reset value = xxxxxxxx

Bit	Name	Function
7	iswdet	Sync Word Detected. When a sync word is detected this bit will be set to 1.
6	ipreaval	Valid Preamble Detected. When a preamble is detected this bit will be set to 1.
5	ipreainval	Invalid Preamble Detected. When the preamble is not found within a period of time set by the invalid preamble detection threshold in Register 54h, this bit will be set to 1.
4	irssi	RSSI. When RSSI level exceeds the programmed threshold this bit will be set to 1.
3	iwut	Wake-Up-Timer. On the expiration of programmed wake-up timer this bit will be set to 1.
2	ilbd	Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled.
1	ichiprdy	Chip Ready (XTAL). When a chip ready event has been detected this bit will be set to 1.
0	ipor	Power-on-Reset (POR). When the chip detects a Power on Reset above the desired setting this bit will be set to 1.

When any of the Interrupt/Status Register 2 bits change state from 0 to 1 the control block will notify the microcontroller by setting the nIRQ pin LOW if it is enabled in the Interrupt Enable 2 register. The nIRQ pin will go to HIGH and all the **enabled** interrupt bits will be cleared when the microcontroller reads this address. If any of these bits is not enabled in the Interrupt Enable 2 register then it becomes a status signal that can be read anytime in the same location and will not be cleared by reading the register.

Table 4. Interrupt or Status 2 Bit Set/Clear Description

Bit	Status Name	Set/Clear Conditions
7	iswdet	Goes high once the Sync Word is detected. Goes low once we are done receiving the current packet.
6	ipreaval	Goes high once the preamble is detected. Goes low once the sync is detected or the RX wait for the sync times-out.
5	ipreainval	Self cleaning, user should use this as an interrupt source rather than a status.
4	irssi	Should remain high as long as the RSSI value is above programmed threshold level
3	iwut	Wake time timer interrupt. Use as an interrupt, not as a status.
2	ilbd	Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced.
1	ichiprdy	Chip ready goes high once we enable the xtal, TX or RX and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.
0	ipor	Power on status.

Table 5. Detailed Description of Status Registers when not Enabled as Interrupts

Bit	Status Name	Set/Clear Conditions
7	iswdet	Goes high once the Sync Word is detected. Goes low once we are done receiving the current packet.
6	ipreaval	Goes high once the preamble is detected. Goes low once the sync is detected or the RX wait for the sync times-out.
5	ipreainval	Self cleaning, user should use this as an interrupt source rather than a status.
4	irssi	Should remain high as long as the RSSI value is above programmed threshold level
3	iwut	Wake time timer interrupt. Use as an interrupt, not as a status.
2	ilbd	Low Battery Detect. When a low battery event is been detected this bit will be set to 1. This interrupt event is saved even if it is not enabled by the mask register bit and causes an interrupt after it is enabled. Probably the status is cleared once the battery is replaced.
1	ichiprdy	Chip ready goes high once we enable the xtal, TX or RX, and a settling time for the Xtal clock elapses. The status stay high unless we go back to Idle mode.
0	ipor	Power on status.

AN440

Register 05h. Interrupt Enable 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enfferr	entxffafull	entxffaem	enrxffafull	enext	enpksent	enpkvalid	encrcerror
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function
7	enfferr	Enable FIFO Underflow/Overflow. When set to 1 the FIFO Underflow/Overflow interrupt will be enabled.
6	entxffafull	Enable TX FIFO Almost Full. When set to 1 the TX FIFO Almost Full interrupt will be enabled.
5	entxffaem	Enable TX FIFO Almost Empty. When set to 1 the TX FIFO Almost Empty interrupt will be enabled.
4	enrxffafull	Enable RX FIFO Almost Full. When set to 1 the RX FIFO Almost Full interrupt will be enabled.
3	enext	Enable External Interrupt. When set to 1 the External Interrupt will be enabled.
2	enpksent	Enable Packet Sent. When ipksent = 1 the Packet Sense Interrupt will be enabled.
1	enpkvalid	Enable Valid Packet Received. When ipkvalid = 1 the Valid Packet Received Interrupt will be enabled.
0	encrcerror	Enable CRC Error. When set to 1 the CRC Error interrupt will be enabled.

Register 06h. Interrupt Enable 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 00000011

Bit	Name	Function
7	enswdet	Enable Sync Word Detected. When mpreadet =1 the Preamble Detected Interrupt will be enabled.
6	enpreaval	Enable Valid Preamble Detected. When mpreadet =1 the Valid Preamble Detected Interrupt will be enabled.
5	enpreainval	Enable Invalid Preamble Detected. When mpreadet =1 the Invalid Preamble Detected Interrupt will be enabled.
4	enrssi	Enable RSSI. When set to 1 the RSSI Interrupt will be enabled.
3	enwut	Enable Wake-Up Timer. When set to 1 the Wake-Up Timer interrupt will be enabled.
2	enlbd	Enable Low Battery Detect. When set to 1 the Low Battery Detect interrupt will be enabled.
1	enchiprdy	Enable Chip Ready (XTAL). When set to 1 the Chip Ready interrupt will be enabled.
0	enpor	Enable POR. When set to 1 the POR interrupt will be enabled.

AN440

Register 07h. Operating Mode and Function Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	swres	enlbd	enwt	x32ksel	txon	rxon	pllon	xton
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00000001

Bit	Name	Function
7	swres	Software Register Reset Bit. This bit may be used to reset all registers simultaneously to a DEFAULT state, without the need for sequentially writing to each individual register. The RESET is accomplished by setting swres = 1. This bit will be automatically cleared.
6	enlbd	Enable Low Battery Detect. When this bit is set to 1 the Low Battery Detector circuit and threshold comparison will be enabled.
5	enwt	Enable Wake-Up-Timer. Enabled when enwt = 1. If the Wake-up-Timer function is enabled it will operate in any mode and notify the microcontroller through the GPIO interrupt when the timer expires.
4	x32ksel	32,768 kHz Crystal Oscillator Select. 0: RC oscillator 1: 32 kHz crystal
3	txon	TX on in Manual Transmit Mode. Automatically cleared in FIFO mode once the packet is sent. Transmission can be aborted during packet transmission, however, when no data has been sent yet, transmission can only be aborted after the device is programmed to "unmodulated carrier" ("Register 71h. Modulation Mode Control 2").
2	rxon	RX on in Manual Receiver Mode. Automatically cleared if Multiple Packets config. is disabled and a valid packet received.
1	pllon	TUNE Mode (PLL is ON). When pllon = 1 the PLL will remain enabled in Idle State. This will for faster turn-around time at the cost of increased current consumption in Idle State.
0	xton	READY Mode (Xtal is ON).

Register 08h. Operating Mode and Function Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	antdiv[2:0]			rxmpk	autotx	enldm	ffclrx	ffclrtx
Type	R/W			R/W	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function																																																		
7:5	antdiv[2:0]	<p>Enable Antenna Diversity. The GPIO must be configured for Antenna Diversity for the algorithm to work properly.</p> <table> <thead> <tr> <th></th> <th>RX/TX state</th> <th colspan="3">non RX/TX state</th> </tr> <tr> <th></th> <th>GPIO Ant1</th> <th>GPIO Ant2</th> <th>GPIO Ant1</th> <th>GPIO Ant2</th> </tr> </thead> <tbody> <tr> <td>000:</td> <td>0</td> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>001:</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>010:</td> <td>0</td> <td>1</td> <td>1</td> <td>1</td> </tr> <tr> <td>011:</td> <td>1</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>100:</td> <td>antenna diversity algorithm</td> <td>0</td> <td>0</td> <td></td> </tr> <tr> <td>101:</td> <td>antenna diversity algorithm</td> <td>1</td> <td>1</td> <td></td> </tr> <tr> <td>110:</td> <td>ant. div. algorithm in beacon mode</td> <td>0</td> <td>0</td> <td></td> </tr> <tr> <td>111:</td> <td>ant. div. algorithm in beacon mode</td> <td>1</td> <td>1</td> <td></td> </tr> </tbody> </table>		RX/TX state	non RX/TX state				GPIO Ant1	GPIO Ant2	GPIO Ant1	GPIO Ant2	000:	0	1	0	0	001:	1	0	0	0	010:	0	1	1	1	011:	1	0	1	1	100:	antenna diversity algorithm	0	0		101:	antenna diversity algorithm	1	1		110:	ant. div. algorithm in beacon mode	0	0		111:	ant. div. algorithm in beacon mode	1	1	
	RX/TX state	non RX/TX state																																																		
	GPIO Ant1	GPIO Ant2	GPIO Ant1	GPIO Ant2																																																
000:	0	1	0	0																																																
001:	1	0	0	0																																																
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110:	ant. div. algorithm in beacon mode	0	0																																																	
111:	ant. div. algorithm in beacon mode	1	1																																																	
4	rxmpk	<p>RX Multi Packet. When the chip is selected to use FIFO Mode (dtmod[1:0]) and RX Packet Handling (enpacrx) then it will fill up the FIFO with multiple valid packets if this bit is set, otherwise the transceiver will automatically leave the RX State after the first valid packet has been received.</p>																																																		
3	autotx	<p>Automatic Transmission. When autotx = 1 the transceiver will enter automatically TX State when the FIFO is almost full. When the FIFO is empty it will automatically return to the Idle State.</p>																																																		
2	enldm	<p>Enable Low Duty Cycle Mode. If this bit is set to 1 then the chip turns on the RX regularly. The frequency should be set in the Wake-Up Timer Period register, while the minimum ON time should be set in the Low-Duty Cycle Mode Duration register. The FIFO mode should be enabled also.</p>																																																		
1	ffclrx	<p>RX FIFO Reset/Clear. This has to be a two writes operation: Setting ffclrx =1 followed by ffclrx = 0 will clear the contents of the RX FIFO.</p>																																																		
0	ffclrtx	<p>TX FIFO Reset/Clear. This has to be a two writes operation: Setting ffclrtx =1 followed by ffclrtx = 0 will clear the contents of the TX FIFO.</p>																																																		

AN440

Register 09h. 30 MHz Crystal Oscillator Load Capacitance

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	xtalshft	xlc[6:0]						
Type	R/W				R/W			

Reset value = 01111111

Bit	Name	Function
7	xtalshft	Additional capacitance to course shift the frequency if xlc[6:0] is not sufficient. Not binary with xlc[6:0].
6:0	xlc[6:0]	Tuning Capacitance for the 30 MHz XTAL.

Register 0Ah. Microcontroller Output Clock

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		clk[1:0]		enlfc	mclk[2:0]		
Type	R		R/W		R/W	R/W		

Reset value = xx000110

Bit	Name	Function
7:6	Reserved	Reserved.
5:4	clk[1:0]	<p>Clock Tail. If enlfc = 0 then it can be useful to provide a few extra cycles for the microcontroller to complete its operation. Setting the clk[1:0] register will provide the addition cycles of the clock before it shuts off.</p> <p>00: 0 cycle 01: 128 cycles 10: 256 cycles 11: 512 cycles</p>
3	enlfc	<p>Enable Low Frequency Clock. When enlfc = 1 and the chip is in Sleep mode then the 32.768 kHz clock will be provided to the microcontroller no matter what the selection of mclk[2:0] is. For example if mclk[2:0] = '000', 30 MHz will be available through the GPIO to output to the microcontroller in all Idle, TX, or RX states. When the chip is commanded to Sleep mode the 30 MHz clock will become 32.768 kHz.</p>
2:0	mclk[2:0]	<p>Microcontroller Clock. Different clock frequencies may be selected for configurable GPIO clock output. All clock frequencies are created by dividing the XTAL except for the 32 kHz clock which comes directly from the 32 kHz RC Oscillator. The mclk[2:0] setting is only valid when xton = 1 except the 111.</p> <p>000: 30 MHz 001: 15 MHz 010: 10 MHz 011: 4 MHz 100: 3 MHz 101: 2 MHz 110: 1 MHz 111: 32.768 kHz</p>

AN440

Register 0Bh. GPIO Configuration 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gpiodrv0[1:0]		pup0	gpio0[4:0]				
Type	R/W		R/W	R/W				

Reset value = 00000000

Bit	Name	Function
7:6	gpiodrv0[1:0]	GPIO Driving Capability Setting.
5	pup0	Pullup Resistor Enable on GPIO0. When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
4:0	gpio0[4:0]	GPIO0 Pin Function Select. 00000: Power-On-Reset (output) 00001: Wake-Up Timer: 1 when WUT has expired (output) 00010: Low Battery Detect: 1 when battery is below threshold setting (output) 00011: Direct Digital Input 00100: External Interrupt, falling edge (input) 00101: External Interrupt, rising edge (input) 00110: External Interrupt, state change (input) 00111: ADC Analog Input 01000: Reserved (Analog Test N Input) 01001: Reserved (Analog Test P Input) 01010: Direct Digital Output 01011: Reserved (Digital Test Output) 01100: Reserved (Analog Test N Output) 01101: Reserved (Analog Test P Output) 01110: Reference Voltage (output) 01111: TX/RX Data CLK output to be used in conjunction with TX/RX Data pin (output) 10000: TX Data input for direct modulation (input) 10001: External Retransmission Request (input) 10010: TX State (output) 10011: TX FIFO Almost Full (output) 10100: RX Data (output) 10101: RX State (output) 10110: RX FIFO Almost Full (output) 10111: Antenna 1 Switch used for antenna diversity (output) 11000: Antenna 2 Switch used for antenna diversity (output) 11001: Valid Preamble Detected (output) 11010: Invalid Preamble Detected (output) 11011: Sync Word Detected (output) 11100: Clear Channel Assessment (output) 11101: VDD else : GND

Register 0Ch. GPIO Configuration 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gpiodrv1[1:0]		pup1	gpio1[4:0]				
Type	R/W		R/W	R/W				

Reset value = 00000000

Bit	Name	Function
7:6	gpiodrv1[1:0]	GPIO Driving Capability Setting.
5	pup1	Pullup Resistor Enable on GPIO1. When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
4:0	gpio1[4:0]	GPIO1 Pin Function Select. 00000: Inverted Power-On-Reset (output) 00001: Wake-Up Timer: 1 when WUT has expired (output) 00010: Low Battery Detect: 1 when battery is below threshold setting (output) 00011: Direct Digital Input 00100: External Interrupt, falling edge (input) 00101: External Interrupt, rising edge (input) 00110: External Interrupt, state change (input) 00111: ADC Analog Input 01000: Reserved (Analog Test N Input) 01001: Reserved (Analog Test P Input) 01010: Direct Digital Output 01011: Reserved (Digital Test Output) 01100: Reserved (Analog Test N Output) 01101: Reserved (Analog Test P Output) 01110: Reference Voltage (output) 01111: TX/RX Data CLK output to be used in conjunction with TX/RX Data pin (output) 10000: TX Data input for direct modulation (input) 10001: External Retransmission Request (input) 10010: TX State (output) 10011: TX FIFO Almost Full (output) 10100: RX Data (output) 10101: RX State (output) 10110: RX FIFO Almost Full (output) 10111: Antenna 1 Switch used for antenna diversity (output) 11000: Antenna 2 Switch used for antenna diversity (output) 11001: Valid Preamble Detected (output) 11010: Invalid Preamble Detected (output) 11011: Sync Word Detected (output) 11100: Clear Channel Assessment (output) 11101: VDD else : GND

AN440

Register 0Dh. GPIO Configuration 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	gpiodrv2[1:0]		pup2	gpio2[4:0]				
Type	R/W		R/W	R/W				

Reset value = 00000000

Bit	Name	Function
7:6	gpiodrv2[1:0]	GPIO Driving Capability Setting.
5	pup2	Pullup Resistor Enable on GPIO2. When set to 1 the a 200 kΩ resistor is connected internally between VDD and the pin if the GPIO is configured as a digital input.
4:0	gpio2[4:0]	GPIO2 Pin Function Select. 00000: Microcontroller Clock 00001: Wake-Up Timer: 1 when WUT has expired (output) 00010: Low Battery Detect: 1 when battery is below threshold setting (output) 00011: Direct Digital Input 00100: External Interrupt, falling edge (input) 00101: External Interrupt, rising edge (input) 00110: External Interrupt, state change (input) 00111: ADC Analog Input 01000: Reserved (Analog Test N Input) 01001: Reserved (Analog Test P Input) 01010: Direct Digital Output 01011: Reserved (Digital Test Output) 01100: Reserved (Analog Test N Output) 01101: Reserved (Analog Test P Output) 01110: Reference Voltage (output) 01111: TX/RX Data CLK output to be used in conjunction with TX/RX Data pin (output) 10000: TX Data input for direct modulation (input) 10001: External Retransmission Request (input) 10010: TX State (output) 10011: TX FIFO Almost Full (output) 10100: RX Data (output) 10101: RX State (output) 10110: RX FIFO Almost Full (output) 10111: Antenna 1 Switch used for antenna diversity (output) 11000: Antenna 2 Switch used for antenna diversity (output) 11001: Valid Preamble Detected (output) 11010: Invalid Preamble Detected (output) 11011: Sync Word Detected (output) 11100: Clear Channel Assessment (output) 11101: VDD else : GND

Register 0Eh. I/O Port Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	extitst[2]	extitst[1]	extitst[0]	itsdo	dio2	dio1	dio0
Type	R	R	R	R	R/W	R/W	R/W	R/W

Reset value = 00000000

Bit	Name	Function
7	Reserved	Reserved.
6	extitst[2]	External Interrupt Status. If the GPIO2 is programmed to be external interrupt sources then the status can be read here.
5	extitst[1]	External Interrupt Status. If the GPIO1 is programmed to be external interrupt sources then the status can be read here.
4	extitst[0]	External Interrupt Status. If the GPIO0 is programmed to be external interrupt sources then the status can be read here.
3	itsdo	Interrupt Request Output on the SDO Pin. nIRQ output is present on the SDO pin if this bit is set and the nSEL input is inactive (high).
2	dio2	Direct I/O for GPIO2. If the GPIO2 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO2 is configured to be a direct input then the value of the pin can be read here.
1	dio1	Direct I/O for GPIO1. If the GPIO1 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO1 is configured to be a direct input then the value of the pin can be read here.
0	dio0	Direct I/O for GPIO0. If the GPIO0 is configured to be a direct output then the value on the GPIO pin can be set here. If the GPIO0 is configured to be a direct input then the value of the pin can be read here.

AN440

Register 0Fh. ADC Configuration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adcstart/ adcdone	adcsel[2:0]			adcref[1:0]		adcgain[1:0]	
Type	R/W	R/W			R/W		R/W	

Reset value = 00000000

Bit	Name	Function
7	adcstart/adc-done	ADC Measurement Start Bit. Reading this bit gives 1 if the ADC measurement cycle has been finished.
6:4	adcsel[2:0]	ADC Input Source Selection. The internal 8-bit ADC input source can be selected as follows: 000: Internal Temperature Sensor 001: GPIO0, single-ended 010: GPIO1, single-ended 011: GPIO2, single-ended 100: GPIO0(+) – GPIO1(-), differential 101: GPIO1(+) – GPIO2(-), differential 110: GPIO0(+) – GPIO2(-), differential 111: GND
3:2	adcref[1:0]	ADC Reference Voltage Selection. The reference voltage of the internal 8-bit ADC can be selected as follows: 0X: bandgap voltage (1.2 V) 10: VDD/3 11: VDD/2
1:0	adcgain[1:0]	ADC Sensor Amplifier Gain Selection. The full scale range of the internal 8-bit ADC in differential mode (see adcsel) can be set as follows: adcref[0] = 0: adcref[0] = 1: FS = 0.014 x (adcgain[1:0] + 1) x VDD FS = 0.021 x (adcgain[1:0] + 1) x VDD

Register 10h. ADC Sensor Amplifier Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				adcoffs[3:0]			
Type	R				R/W			

Reset value = xxxx0000

Bit	Name	Function
7:4	Reserved	Reserved.
3:0	adcoffs[3:0]	ADC Sensor Amplifier Offset*.

***Note:** The offset can be calculated as $\text{Offset} = \text{adcoffs}[2:0] \times \text{VDD}/1000$; MSB = $\text{adcoffs}[3]$ = Sign bit.

Register 11h. ADC Value

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adc[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	adc[7:0]	Internal 8 bit ADC Output Value.

AN440

Register 12h. Temperature Sensor Calibration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	tsrange[1:0]		entsoffs	entstrim	tstrim[3:0]			
Type	R/W		R/W	R/W	R/W			

Reset value = 00100000

Bit	Name	Function
7:6	tsrange[1:0]	Temperature Sensor Range Selection. (FS range is 0..1024 mV) 00: -40 °C .. 64 °C (full operating range), with 0.5 °C resolution (1 LSB in the 8-bit ADC) 01: -40 °C .. 85 °C, with 1 °C resolution (1 LSB in the 8-bit ADC) 11: 0 °C .. 85 °C, with 0.5 °C resolution (1 LSB in the 8-bit ADC) 10: -40 °F .. 216 °F, with 1 °F resolution (1 LSB in the 8-bit ADC)
5	entsoffs	Temperature Sensor Offset to Convert from K to °C.
4	entstrim	Temperature Sensor Trim Enable.
3:0	tstrim[3:0]	Temperature Sensor Trim Value.

Register 13h. Temperature Value Offset

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	tvoffs[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	tvoffs[7:0]	Temperature Value Offset. This value is added to the measured temperature value. (MSB, tvoffs[8]: sign bit).

Note: If a new configuration is needed (e.g., for the WUT or the LDC), proper functionality is required. The function must first be disabled, then the settings changed, then enabled back on.

Register 14h. Wake-Up Timer Period 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			wtr[4:0]				
Type	R/W			R/W				

Reset value = xxx00011

Bit	Name	Function
7:5	Reserved	Reserved.
4:0	wtr[4:0]	Wake Up Timer Exponent (R) Value*. Maximum value for R is decimal 20. A value greater than 20 will yield a result as if 20 were written. R Value = 0 can be written here.
* Note: The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R)/32.768$ ms. R = 0 is allowed, and the maximum value for R is decimal 20. A value greater than 20 will result in the same as if 20 was written.		

Register 15h. Wake-Up Timer Period 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[15:8]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	wtm[15:8]	Wake Up Timer Mantissa (M) Value*.
* Note: The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R)/32.768$ ms.		

Register 16h. Wake-Up Timer Period 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[7:0]							
Type	R/W							

Reset value = 00000001

Bit	Name	Function
7:0	wtm[7:0]	Wake Up Timer Mantissa (M) Value*. M[7:0] = 0 is not valid here. Write at least decimal 1.
* Note: The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R)/32.768$ ms.		

AN440

Register 17h. Wake-Up Timer Value 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[15:8]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	wtm[15:8]	Wake Up Timer Current Mantissa (M) Value*.

***Note:** The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R)/32.768$ ms.

Register 18h. Wake-Up Timer Value 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	wtm[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	wtm[7:0]	Wake Up Timer Current Mantissa (M) Value*.

***Note:** The period of the wake-up timer can be calculated as $T_{WUT} = (4 \times M \times 2^R)/32.768$ ms.

Register 19h. Low-Duty Cycle Mode Duration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ldc[7:0]							
Type	R/W							

Reset value = 00000001

Bit	Name	Function
7:0	ldc[7:0]	Low-Duty Cycle Mode Duration (LDC)*. If enabled, the LDC will start together when the WUT is supposed to start, and the duration of the LDC is specified by the address 19h and the equation that goes with it. In order for the LDC to work, the LDC value has to be smaller than the M value specified in registers 15h and 16h. LDC = 0 is not allowed here. Write at least decimal 1.

***Note:** The period of the low-duty cycle ON time can be calculated as $T_{LDC_ON} = (4 \times LDC \times 2^R)/32.768$ ms. R is the same as in the wake-up timer setting in "Register 14h. Wake-Up Timer Period 1". The LDC works in conjunction with the WUT. The LDC period must be specified to be smaller than the WUT period. (i.e., the LDC register must be smaller than the M register). The LDC may not be programmed to 0.

Register 1Ah. Low Battery Detector Threshold

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			lbdt[4:0]				
Type	R			R/W				

Reset value = xxx10100

Bit	Name	Function
7:5	Reserved	Reserved.
4:0	lbdt[4:0]	Low Battery Detector Threshold. This threshold is compared to Battery Voltage Level. If the Battery Voltage is less than the threshold the Low Battery Interrupt is set. Default = 2.7 V.*
*Note: The threshold can be calculated as $V_{\text{threshold}} = 1.7 + \text{lbdt} \times 50 \text{ mV}$.		

Register 1Bh. Battery Voltage Level

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			vbat[4:0]				
Type	R			R				

Reset value = xxxxxxxx

Bit	Name	Function
7:5	Reserved	Reserved.
4:0	vbat[4:0]	Battery Voltage Level. The battery voltage is converted by a 5 bit ADC. In Sleep Mode the register is updated in every 1 s. In other states it measures continuously.

Register 1Ch. IF Filter Bandwidth

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	dwn3_bypass	ndec_exp[2:0]			filset[3:0]			
Type	R/W	R/W			R/W			

Reset value = 00000001

Bit	Name	Function
7	dwn3_bypass	Bypass Decimator by 3 (if set).
6:4	ndec_exp[2:0]	IF Filter Decimation Rates.
3:0	filset[3:0]	IF Filter Coefficient Sets. Defaults are for Rb = 40 kbps and Fd = 20 kHz so Bw = 80 kHz.

Register 1Dh. AFC Loop Gearshift Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	afcbd	enafc	afcgearh[2:0]			afcgearl[2:0]		
Type	R/W	R/W	R/W			R/W		

Reset value = 01000100

Bit	Name	Function
7	afcbd	If set, the tolerated AFC frequency error will be halved.
6	enafc	AFC Enable.
5:3	afcgearh[2:0]	AFC High Gear Setting.
2:0	afcgearl[2:0]	AFC Low Gear Setting.

Register 1Eh. AFC Timing Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	swait_timer[1:0]		shwait[2:0]			anwait[2:0]		
Type	R		R/W			R/W		

Reset value = xx001010

Bit	Name	Function
7:6	swait_timer[1:0]	Short Wait RSSI Timer. The second phase RSSI waiting timer offset.
5:3	shwait[2:0]	Short Wait Periods after AFC Correction. Used before preamble is detected. Short wait = (RegValue + 1) x 2T _b . If set to 0 then no AFC correction will occur before preamble detect, i.e. AFC will be disabled.
2:0	anwait[2:0]	Antenna Switching Wait Time. Value corresponds to number of bits.

Register 1Fh. Clock Recovery Gearshift Override

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		crfast[2:0]			crslow[2:0]		
Type	R/W		R/W			R/W		

Reset value = 00000011

Bit	Name	Function
7:6	Reserved	Reserved.
5:3	crfast[2:0]	Clock Recovery Fast Gearshift Value.
2:0	crslow[2:0]	Clock Recovery Slow Gearshift Value.

The gear-shift register controls BCR loop gain. Before the preamble is detected, BCR loop gain is as follows:

$$BCRLoopGain = \frac{crgain}{2^{crfast}}$$

Once the preamble is detected, internal state machine automatically shift BCR loop gain to the following:

$$BCRLoopGain = \frac{crgain}{2^{crslow}}$$

crfast = 3'b000 and crslow = 3'b101 are recommended for most applications. The value of "crslow" should be greater than "crfast".

Register 20h. Clock Recovery Oversampling Rate

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rxosr[7:0]							
Type	R/W							

Reset value = 01100100

Bit	Name	Function
7:0	rxosr[7:0]	Oversampling Rate. 3 LSBs are the fraction, default = 0110 0100 = 12.5 clock cycles per data bit

The oversampling rate can be calculated as $rxosr = 500 \text{ kHz} / (2^{ndec_exp} \times RX_DR)$. The $ndec_exp$ and the $dwn3_bypass$ values found at Address: 1Ch-IF Filter Bandwidth register together with the receive data rate (Rb) are the parameters needed to calculate $rxosr$:

$$rxosr = \frac{500 \times (1 + 2 \times dwn3_bypass)}{2^{ndec_exp-3} \times Rb \times (1 + enmanch)}$$

The Rb unit used in this equation is in kbps. The $enmanch$ is the Manchester Coding parameter (see Reg. 70h, $enmach$ is 1 when Manchester coding is enabled, $enmanch$ is 0 when disabled). The number found in the equation should be rounded to an integer. The integer can be translated to a hexadecimal.

For optimal modem performance it is recommended to set the $rxosr$ to at least 8. A higher $rxosr$ can be obtained by choosing a lower value for $ndec_exp$ or enable $dwn3_bypass$. A correction in $filset$ might be needed to correct the channel select bandwidth to the desired value. Note that when $ndec_exp$ or $dwn3_bypass$ are changed the related parameters ($rxosr$, $ncoff$ and $crgain$) need to be updated.

Register 21h. Clock Recovery Offset 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rxosr[10:8]			stallctrl	ncoff[19:16]			
Type	R/W			R/W	R/W			

Reset value = 00000001

Bit	Name	Function
7:5	rxosr[10:8]	Oversampling Rate. Upper bits.
4	stallctrl	Used for BCR Purposes.
3:0	ncoff[19:16]	NCO Offset. See formula above.

The offset can be calculated as follows:

$$ncoff = \frac{Rb \times (1 + enmanch) \times 2^{20+ndec_exp}}{500 \times (1 + 2 \times dwn3_bypass)}$$

The default values for register 20h to 23h gives 40 kbps RX_DR with Manchester coding is disenabled.

Register 22h. Clock Recovery Offset 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ncoff[15:8]							
Type	R/W							

Reset value = 01000111

Bit	Name	Function
7:0	ncoff[15:8]	NCO Offset. See formula above.

Register 23h. Clock Recovery Offset 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ncoff[7:0]							
Type	R/W							

Reset value = 10101110

Bit	Name	Function
7:0	ncoff[7:0]	NCO Offset. See formula above

Register 24h. Clock Recovery Timing Loop Gain 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved			rxncocomp	cgainx2	crgain[10:8]		
Type	R/W			R/W	R/W	R/W		

Reset value = 00000010

Bit	Name	Function
7:5	Reserved	Reserved.
4	rxncocomp	Receive Compensation Enable for High Data Rate Offset.
3	cgainx2	Multiplying the CR Gain by 2.
2:0	crgain[10:8]	Clock Recovery Timing Loop Gain.

The loop gain can be calculated as follows:

$$crgain = 2 + \frac{2^{16} \times (1 + enmanch) \times Rb}{rxosr \times Fd}$$

Register 25h. Clock Recovery Timing Loop Gain 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	crgain[7:0]							
Type	R/W							

Reset value = 10001111

Bit	Name	Function
7:0	crgain[7:0]	Clock Recovery Timing Loop Gain.

Register 26h. Received Signal Strength Indicator

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rssi[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	rssi[7:0]	Received Signal Strength Indicator Value.

Register 27h. RSSI Threshold for Clear Channel Indicator

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rssith[7:0]							
Type	R/W							

Reset value = 00011110

Bit	Name	Function
7:0	rssith[7:0]	RSSI Threshold. Interrupt is set if the RSSI value is above this threshold.

Register 28h. Antenna Diversity 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adrssi[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	adrssi[7:0]	Measured RSSI Value on Antenna 1.

Register 29h. Antenna Diversity 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	adrssi2[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	adrssi2[7:0]	Measured RSSI Value on Antenna 2.

Register 2Ah. AFC Limiter

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Afclim[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	Afclim[7:0]	AFC Limiter. AFC limiter value.

For the following registers (addresses 2Bh and 2Ch), use the following equation:

$$ook \ \underline{cnt} \ val = \frac{3 \times 500[\text{kHz}]}{R_b \times (enmanch + 1)}$$

where R_b 's unit is in kHz and "enmanch" is the Manchester Enable bit (found at address 71h bit [1]).

Therefore, the minimal data rate that this register can support without Manchester is 0.366 kbps.

Register 2Bh. AFC Correction (LSBs)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	afc_corr[9:2]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	afc_corr[9:2]	AFC Correction Values. AFC loop correction values [9:2] (MSBs only). Values are updated once, after sync word is found during receiving. See also address 2Ch.

Register 2Ch. OOK Counter Value 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	afc_corr[1:0]		ookfrzen	peakdeten	madeten	ookcnt[10]	ookcnt[9]	ookcnt[8]
Type	R		R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00011000

Bit	Name	Function
7:6	afc_corr[1:0]	AFC Correction Values. AFC loop correction values [1:0] (LSBs). Values are updated once, after sync word is found during receiving. See also address 2Bh.
5	ookfrzen	OOK Freeze. OOK AGC freeze if this bit is set.
4	peakdeten	Peak Detector Enable. Peak detector enable if high.
3	madeten	MA_Enable. MA block enable if high.
2:0	ookcnt[2:0]	OOK Counter [10:8]. OOK counter value MSBs.

Register 2Dh. OOK Counter Value 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ookcnt[7:0]							
Type	R/W							

Reset value = 10111100

Bit	Name	Function
7:0	afc_corr[9:2]	OOK Counter [7:0]. OOK counter value LSBs.

Register 2Eh. Slicer Peak Holder

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	attack[2:0]			decay[3:0]			
Type	R/W	R/W			R/W			

Reset value = 00101100

Bit	Name	Function
7	Reserved	Reserved.
6:4	attack[2:0]	Attack.
3:0	decay[3:0]	Decay.

Register 30h. Data Access Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	enpacrx	lsbfrst	crcdonly	skip2ph	enpactx	encrc	crc[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Reset value = 10001101

Bit	Name	Function
7	enpacrx	Enable Packet RX Handling. If FIFO Mode (dtmod = 10) is being used automatic packet handling may be enabled. Setting enpacrx = 1 will enable automatic packet handling in the RX path. Register 30–4D allow for various configurations of the packet structure. Setting enpacrx = 0 will not do any packet handling in the RX path. It will only receive everything after the sync word and fill up the RX FIFO.
6	lsbfrst	LSB First Enable. The LSB of the data will be transmitted/received first if this bit is set.
5	crcdonly	CRC Data Only Enable. When this bit is set to 1 the CRC is calculated on and checked against the packet data fields only.
4	skip2ph	Skip 2nd Phase of Preamble Detection. If set, we skip the second phase of the preamble detection (under certain conditions) if antenna diversity is enabled.
3	enpactx	Enable Packet TX Handling. If FIFO Mode (dtmod = 10) is being used automatic packet handling may be enabled. Setting enpactx = 1 will enable automatic packet handling in the TX path. Register 30–4D allow for various configurations of the packet structure. Setting enpactx = 0 will not do any packet handling in the TX path. It will only transmit what is loaded to the FIFO.
2	encrc	CRC Enable. Cyclic Redundancy Check generation is enabled if this bit is set.
1:0	crc[1:0]	CRC Polynomial Selection. 00: CCITT 01: CRC-16 (IBM) 10: IEC-16 11: Biacheva

Register 31h. EZMAC[®] Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	rxcrc1	pksrch	pkrx	pkvalid	crcerror	pktx	pksent
Type	R	R	R	R	R	R	R	R

Reset value = 00000000

Bit	Name	Function
7	Reserved	Reserved.
6	rxcrc1	If high, it indicates the last CRC received is all one's. May indicated Transmitter underflow in case of CRC error.
5	pksrch	Packet Searching. When pksrch = 1 the radio is searching for a valid packet.
4	pkrx	Packet Receiving. When pkrx = 1 the radio is currently receiving a valid packet.
3	pkvalid	Valid Packet Received. When a pkvalid = 1 a valid packet has been received by the receiver. (Same bit as in register 03, but reading it does not reset the IRQ)
2	crcerror	CRC Error. When crcerror = 1 a Cyclic Redundancy Check error has been detected. (Same bit as in register 03, but reading it does not reset the IRQ)
1	pktx	Packet Transmitting. When pktx = 1 the radio is currently transmitting a packet.
0	pksent	Packet Sent. A pksent = 1 a packet has been sent by the radio. (Same bit as in register 03, but reading it does not reset the IRQ)

Register 32h. Header Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	bcen[3:0]				hdch[3:0]			
Type	R/W				R/W			

Reset value = 00001100

Bit	Name	Function
7:4	bcen[3:0]	<p>Broadcast Address (FFh) Check Enable.</p> <p>If it is enabled together with Header Byte Check then the header check is OK if the incoming header byte equals with the appropriate check byte <i>or</i> FFh). One hot encoding.</p> <p>0000: No broadcast address enable. 0001: Broadcast address enable for header byte 0. 0010: Broadcast address enable for header byte 1. 0011: Broadcast address enable for header bytes 0 & 1. 0100: ...</p>
3:0	hdch[3:0]	<p>Received Header Bytes to be Checked Against the Check Header Bytes.</p> <p>One hot encoding. The receiver will use hdch[2:0] to know the position of the Header Bytes.</p> <p>0000: No Received Header check 0001: Received Header check for byte 0. 0010: Received Header check for bytes 1. 0011: Received header check for bytes 0 & 1. 0100: ...</p>

Register 33h. Header Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	hdlen[2:0]			fixpklen	syncnlen[1:0]		prealen[8]
Type	R	R/W			R/W	R/W		R/W

Reset value = 00100010

Bit	Name	Function
7	Reserved	Reserved.
6:4	hdlen[2:0]	Header Length. Length of header used if packet handler is enabled for TX/RX (enpactx/rx). Headers are transmitted/received in descending order. 000: No TX/RX header 001: Header 3 010: Header 3 and 2 011: Header 3 and 2 and 1 100: Header 3 and 2 and 1 and 0
3	fixpklen	Fix Packet Length. When fixpklen = 1 the packet length (pklen[7:0]) is not included in the header. When fixpklen = 0 the packet length is included in the header.
2:1	syncnlen[1:0]	Synchronization Word Length. The value in this register corresponds to the number of bytes used in the Synchronization Word. The synchronization word bytes are transmitted/received in descending order. 00: Synchronization Word 3 01: Synchronization Word 3 followed by 2 10: Synchronization Word 3 followed by 2 followed by 1 11: Synchronization Word 3 followed by 2 followed by 1 followed by 0
0	prealen[8]	MSB of Preamble Length. See register Preamble Length.

Register 34h. Preamble Length

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	prealen[7:0]							
Type	R/W							

Reset value = 00001000

Bit	Name	Function
7:0	prealen[7:0]	<p>Preamble Length.</p> <p>The value in the prealen[8:0] register corresponds to the number of nibbles (4 bits) in the packet. For example prealen[8:0] = '000001000' corresponds to a preamble length of 32 bits (8 x 4bits) or 4 bytes. The maximum preamble length is prealen[8:0] = 111111111 which corresponds to a 255 bytes Preamble. Writing 0 will have the same result as if writing 1, which corresponds to one single nibble of preamble.</p>

Register 35h. Preamble Detection Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	preath[4:0]					rssi_offset[2:0]		
Type	R/W					R/W		

Reset value = 00101010

Bit	Name	Function
7:3	preath[4:0]	Number of nibbles processed during detection.
2:0	rssi_offset[2:0]	<p>rssi_offset[2:0]</p> <p>Value added as offset to RSSI calculation. Every increment in this register results in an increment of +4 dB in the RSSI.</p>

Register 36h. Synchronization Word 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[31:24]							
Type	R/W							

Reset value = 00101101

Bit	Name	Function
7:0	sync[31:24]	Synchronization Word 3. 4 th byte of the synchronization word.

Register 37h. Synchronization Word 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[23:16]							
Type	R/W							

Reset value = 11010100

Bit	Name	Function
7:0	sync[23:16]	Synchronization Word 2. 3 rd byte of the synchronization word.

Register 38h. Synchronization Word 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[15:8]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	sync[15:8]	Synchronization Word 1. 2 nd byte of the synchronization word.

Register 39h. Synchronization Word 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	sync[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	sync[7:0]	Synchronization Word 0. 1 st byte of the synchronization word.

Register 3Ah. Transmit Header 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[31:24]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[31:24]	Transmit Header 3. 4 th byte of the header to be transmitted.

Register 3Bh. Transmit Header 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[23:16]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[23:16]	Transmit Header 2. 3 rd byte of the header to be transmitted.

Register 3Ch. Transmit Header 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[15:8]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[15:8]	Transmit Header 1. 2 nd byte of the header to be transmitted.

Register 3Dh. Transmit Header 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txhd[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	txhd[7:0]	Transmit Header 0. 1 st byte of the header to be transmitted.

Register 3Eh. Packet Length

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pklen[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	pklen[7:0]	Packet Length. The value in the pklen[7:0] register corresponds directly to the number of bytes in the Packet. For example pklen[7:0] = '00001000' corresponds to a packet length of 8 bytes. The maximum packet length is pklen[7:0] = '11111111', a 255 byte packet. Writing 0 is possible, in this case we do not send any data in the packet. During RX, if <i>fixpklen</i> = 1, this will specify also the Packet Length for RX mode.

Check Header bytes 3 to 0 are checked against the corresponding bytes in the Received Header if the check is enabled in "Register 31h. EZMAC[®] Status," on page 36.

Register 3Fh. Check Header 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	chhd[31:24]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	chhd[31:24]	Check Header 3. 4 th byte of the check header.

Register 40h. Check Header 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	chhd[23:16]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	chhd[23:16]	Check Header 2. 3 rd byte of the check header.

Register 41h. Check Header 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	chhd[15:8]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	chhd[15:8]	Check Header 1. 2 nd byte of the check header.

Register 42h. Check Header 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	chhd[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	chhd[7:0]	Check Header 0. 1 st byte of the check header.

Header Enable bytes 3 to 0 control which bits of the Check Header bytes are checked against the corresponding bits in the Received Header. Only those bits are compared where the enable bits are set to 1.

Register 43h. Header Enable 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	hden[31:24]							
Type	R/W							

Reset value = 11111111

Bit	Name	Function
7:0	hden[31:24]	Header Enable 3. 4 th byte of the check header.

Register 44h. Header Enable 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	hden[23:16]							
Type	R/W							

Reset value = 11111111

Bit	Name	Function
7:0	hden[23:16]	Header Enable 2. 3 rd byte of the check header.

Register 45h. Header Enable 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	hden[15:8]							
Type	R/W							

Reset value = 11111111

Bit	Name	Function
7:0	hden[15:8]	Header Enable 1. 2 nd byte of the check header.

Register 46h. Header Enable 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	hden[7:0]							
Type	R/W							

Reset value = 11111111

Bit	Name	Function
7:0	hden[7:0]	Header Enable 0. 1 st byte of the check header.

Register 47h. Received Header 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rxhd[31:24]							
Type	R							

Reset value = 00000000

Bit	Name	Function
7:0	rxhd[31:24]	Received Header 3. 4 th byte of the received header.

Register 48h. Received Header 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rxhd[23:16]							
Type	R							

Reset value = 00000000

Bit	Name	Function
7:0	rxhd[23:16]	Received Header 2. 3 rd byte of the received header.

Register 49h. Received Header 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rxhd[15:8]							
Type	R							

Reset value = 00000000

Bit	Name	Function
7:0	rxhd[15:8]	Received Header 1. 2 nd byte of the received header.

Register 4Ah. Received Header 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rxhd[7:0]							
Type	R							

Reset value = 00000000

Bit	Name	Function
7:0	rxhd[7:0]	Received Header 0. 1 st byte of the received header.

Register 4Bh. Received Packet Length

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	rxplen[7:0]							
Type	R							

Reset value = xxxxxxxx

Bit	Name	Function
7:0	rxplen[7:0]	Length Byte of the Received Packet during <i>fixpklen</i> = 0. (Specifies the number of Data bytes in the last received packet) This will be relevant ONLY if <i>fixpklen</i> (address 33h, bit[3]) is low during the receive time. If <i>fixpklen</i> is high, then the number of received Data Bytes can be read from the <i>pklen</i> register (address h3E).

Register 4Fh. ADC8 Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved[7:6]		adc8[5:0]					
Type	R/W		R/W					

Reset value = 00010000

Bit	Name	Function
7:6	Reserved	Reserved.
5:0	adc8[5:0]	ADC8 Control Bits.

Register 60h. Channel Filter Coefficient Address

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				chfiladd[3:0]			
Type	R/W				R/W			

Reset value = 00000000

Bit	Name	Function
7:4	Reserved	Reserved.
3:0	chfiladd[3:0]	Channel Filter Coefficient Look-up Table Address. The address for channel filter coefficients used in the RX path.

Register 62h. Crystal Oscillator/Power-on-Reset Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	pwst[2:0]			clkhyst	enbias2x	enamp2x	bufovr	enbuf
Type	R			R/W	R/W	R/W	R/W	R/W

Reset value = xxx00100

Bit	Name	Function
7:5	pwst[2:0]	Internal Power States of the Chip. LP: 000 RDY: 001 Tune: 011 TX: 010 RX: 111
4	clkhyst	Clock Hysteresis Setting.
3	enbias2x	2 Times Higher Bias Current Enable.
2	enamp2x	2 Times Higher Amplification Enable.
1	bufovr	Output Buffer Enable Override. If set to 1 then the enbuf bit controls the output buffer. 0: output buffer is controlled by the state machine. 1: output buffer is controlled by the enbuf bit.
0	enbuf	Output Buffer Enable. This bit is active only if the bufovr bit is set to 1.

Register 69h. AGC Override 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	sgi	agcen	lnagain	pga[3:0]			
Type	R	R/W	R/W	R/W	R/W			

Reset value = 00100000

Bit	Name	Function
7	Reserved	Reserved.
6	sgi	AGC Loop, Set Gain Increase. If set to 0 then gain increasing will not be allowed. If set to 1 then gain increasing is allowed, default is 0.
5	agcen	Automatic Gain Control Enable. When this bit is set then the result of the control can be read out from bits [4:0], otherwise the gain can be controlled manually by writing into bits [4:0].
4	lnagain	LNA Gain Select. 0 – min. gain = 5 dB 1 – max. gain = 25 dB
3:0	pga[3:0]	PGA Gain Override Value. 000: 0 dB 001: 3 dB 010: 6 dB ... 101: 24 dB max.

Register 6Dh. TX Power

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	papeakval	papeaken	papeak- lvl[1]	papeak- lvl[0]	lna_sw	txpow[2:0]		
Type	R	R/W	R/W	R/W	R/W	R/W		

Reset value = x0011000

Bit	Name	Function
7	papeakval	Reserved.
6	papeaken	PA Peak Detector Value Read Register. Reading a 1 in this register when the papeaken=1 then the PA drain voltage is too high and the match network needs adjusting for optimal efficiency.
5	papeaklvl[1]	PA Peak Detector Enable.
4	papeaklvl[0]	PA Peak Detect Level (direct from register). 00 = 6.5 01 = 7 10 = 7.5 11 = 8 00 = default
3	lna_sw	LNA Switch Controller. If set, lna_sw control from the digital will go high during TX modes, and low during other times. If reset, the digital control signal is low at all times.
2:0	txpow[2:0]	TX Output Power. The output power is configurable from -8 dBm to +13 dBm in ~3 dBm steps. txpow[2:0] = 111 corresponds to +13 dBm and 000 to -8 dBm.

Register 6Eh. TX Data Rate 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txdr[15:8]							
Type	R/W							

Reset value = 00001010

Bit	Name	Function
7:0	txdr[15:8]	Data Rate Upper Byte. See formula above.

The data rate can be calculated as: $TX_DR = 10^3 \times txdr[15:0]/2^{16}$ [kbps] (if address 70[5] = 0) orThe data rate can be calculated as: $TX_DR = 10^3 \times txdr[15:0]/2^{21}$ [kbps] (if address 70[5] = 1)

Register 6Fh. TX Data Rate 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	txdr[7:0]							
Type	R/W							

Reset value = 00111101

Bit	Name	Function
7:0	txdr[7:0]	Data Rate Lower Byte. See formula above. Defaults = 40 kbps.

Register 70h. Modulation Mode Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		txdtrtscale	enphpwdn	manppol	enmaninv	enmanch	enwhite
Type	R		R/W	R/W	R/W	R/W	R/W	R/W

Reset value = 00001100

Bit	Name	Function
7:6	Reserved	Reserved.
5	txdtrtscale	This bit should be set for Data Rates below 30 kbps.
4	enphpwdn	If set, the Packet Handler will be powered down when chip is in low power mode.
3	manppol	Manchester Preamble Polarity (will transmit a series of 1 if set, or series of 0 if reset). This bit affects only the transmitter side, not the receiver. This is valid only if Manchester Mode is enabled.
2	enmaninv	Manchester Data Inversion is Enabled if this bit is set. When this bit is low, a 10 pair is considered a Manchester 0, and a 01 pair as a Manchester 1. By setting this bit, do the opposite: every 10 will be considered as a 1, and every 01 will be considered as a 0. This function is relevant only if the Manchester mode is enabled.
1	enmanch	Manchester Coding is Enabled if this bit is set. What Manchester coding does is to replace a single high bit (1) with two bits starting with low followed by high (01) and a low bit (0) with a high bit followed by a low bit (10). When Manchester is enabled, please configure as well the enmaninv at 70h bit [2] since it influences the Manchester encoding/decoding process.
0	enwhite	Data Whitening is Enabled if this bit is set.

Register 71h. Modulation Mode Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	trclk[1:0]		dtmod[1:0]		eninv	fd[8]	modtyp[1:0]	
Type	R/W		R/W		R/W	R/W	R/W	

Reset value = 00000000

Bit	Name	Function
7:6	trclk[1:0]	TX Data Clock Configuration. 00: No TX Data CLK is available (asynchronous mode – Can only work with modulations FSK or OOK). 01: TX Data CLK is available via the GPIO (one of the GPIO's should be programmed as well). 10: TX Data CLK is available via the SDO pin. 11: TX Data CLK is available via the nIRQ pin.
5:4	dtmod[1:0]	Modulation Source. 00: Direct Mode using TX_Data function via the GPIO pin (one of the GPIO's should be programmed accordingly as well) 01: Direct Mode using TX_Data function via the SDI pin (only when nSEL is high) 10: FIFO Mode 11: PN9 (internally generated)
3	eninv	Invert TX and RX Data.
2	fd[8]	MSB of Frequency Deviation Setting, see "Register 72h. Frequency Deviation".
1:0	modtyp[1:0]	Modulation Type. 00: Unmodulated carrier 01: OOK 10: FSK 11: GFSK (enable TX Data CLK (trclk[1:0]) when direct mode is used)

The frequency deviation can be calculated: $Fd = 625 \text{ Hz} \times fd[8:0]$.

Register 72h. Frequency Deviation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fd[7:0]							
Type	R/W							

Reset value = 00100000

Bit	Name	Function
7:0	fd[7:0]	Frequency Deviation Setting. See formula above.

Note: It's recommended to use modulation index of 1 or higher (maximum allowable modulation index is 32). The modulation index is defined by $2F_N/F_R$ where F_D is the deviation and R_B is the data rate. When Manchester coding is enabled the modulation index is defined by F_D/R_B .

Register 73h. Frequency Offset 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fo[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	fo[7:0]	Frequency Offset Setting. The frequency offset can be calculated as $\text{Offset} = 156.25 \text{ Hz} \times (\text{hbssel} + 1) \times \text{fo}[7:0]$. fo[9:0] is a two's complement value. Reading from this register will give the AFC correction last results, not this register value.

Reading from this register will give the AFC correction last results, not this register value.

Register 74h. Frequency Offset 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						fo[9:8]	
Type	R						R/W	

Reset value = 00000000

Bit	Name	Function
7:2	Reserved	Reserved.
1:0	fo[9:8]	Upper Bits of the Frequency Offset Setting. fo[9] is the sign bit. The frequency offset can be calculated as Offset = 156.25 Hz x (hbssel + 1) x fo[7:0]. fo[9:0] is a twos complement value. Reading from this register will give the AFC correction last results, not this register value.

Register 75h. Frequency Band Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	sbsel	hbssel	fb[4:0]				
Type	R	R/W	R/W	R/W				

Reset value = 01110101

Bit	Name	Function
7	Reserved	Reserved.
6	sbsel	Side Band Select.
5	hbssel	High Band Select. Setting hbssel = 1 will choose the frequency range from 480–960 MHz (high bands). Setting hbssel = 0 will choose the frequency range from 240–479.9 MHz (low bands).
4:0	fb[4:0]	Frequency Band Select. Every increment corresponds to a 10 MHz Band for the Low Bands and a 20 MHz Band for the High Bands. Setting fb[4:0] = 00000 corresponds to the 240–250 MHz Band for hbssel = 0 and the 480–500 MHz Band for hbssel = 1. Setting fb[4:0] = 00001 corresponds to the 250–260 MHz Band for hbssel = 0 and the 500–520 MHz Band for hbssel = 1.

The RF carrier frequency can be calculated as follows:

$$f_{\text{carrier}} = (f_b + 24 + (f_c + f_o) / 64000) \times 10000 \times (\text{hb_ssel} + 1) + (f_{\text{hch}} \times f_{\text{hs}} \times 10) \text{ [kHz]},$$

where parameters f_c , f_o , f_b and hb_sel come from registers 73h–77h. Parameters f_{hch} and f_{hs} come from register 79h and 7Ah.

Register 76h. Nominal Carrier Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fc[15:8]							
Type	R/W							

Reset value = 10111011

Bit	Name	Function
7:0	fc[15:8]	Nominal Carrier Frequency Setting. See formula above.

Register 77h. Nominal Carrier Frequency

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fc[7:0]							
Type	R/W							

Reset value = 10000000

Bit	Name	Function
7:0	fc[7:0]	Nominal Carrier Frequency Setting. See formula above.

Register 79h. Frequency Hopping Channel Select

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fhch[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	fhch[7:0]	Frequency Hopping Channel Number.

Register 7Ah. Frequency Hopping Step Size

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fhs[7:0]							
Type	R/W							

Reset value = 00000000

Bit	Name	Function
7:0	fhs[7:0]	Frequency Hopping Step Size in 10 kHz Increments. See formula for the nominal carrier frequency at "Register 76h. Nominal Carrier Frequency".

Register 7Ch. TX FIFO Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		txafthr[5:0]					
Type	R/W			R/W				

Reset value = 00110111

Bit	Name	Function
7:6	Reserved	Reserved.
5:0	txafthr[5:0]	TX FIFO Almost Full Threshold.

Register 7Dh. TX FIFO Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		txfaethr[5:0]					
Type	R/W			R/W				

Reset value = 00000100

Bit	Name	Function
7:6	Reserved	Reserved.
5:0	txfaethr[5:0]	TX FIFO Almost Empty Threshold.

Register 7Eh. RX FIFO Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		rxafthr[5:0]					
Type	R/W			R/W				

Reset value = 00110111

Bit	Name	Function
7:6	Reserved	Reserved.
5:0	rxafthr[5:0]	RX FIFO Almost Full Threshold.

Register 7Fh. FIFO Access

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	fifod[7:0]							
Type	R/W							

Reset value = NA

Bit	Name	Function
7:0	fifod[7:0]	<p>FIFO Data.</p> <p>A Write (R/W = 1) to this Address will begin a Burst Write to the TX FIFO. The FIFO will be loaded in the same manner as a Burst SPI Write but the SPI address will not be incremented. To conclude the TX FIFO Write the SEL pin should be brought HIGH. A Read (R/W = 0) to this address will begin a burst read of the RX FIFO, in the same manner.</p>

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